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|---|---|
| **Titre:** Title: | Circuit techniques for low-voltage deep submicron CMOS analog-to-digital converters |
| **Auteur:** Author: | Christian Jésus Bayodé Fayomi |
| **Date:** | 2003 |
| **Type:** | Mémoire ou thèse / Dissertation or Thesis |
| **Référence:** Citation: | Fayomi, C. J. B. (2003). Circuit techniques for low-voltage deep submicron CMOS analog-to-digital converters [Ph.D. thesis, École Polytechnique de Montréal]. PolyPublie. https://publications.polymtl.ca/7169/ |

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UNIVERSITÉ DE MONTRÉAL

# CIRCUIT TECHNIQUES FOR LOW-VOLTAGE DEEP SUBMICRON CMOS ANALOG-TO-DIGITAL CONVERTERS

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ÉCOLE POLYTECHNIQUE DE MONTRÉAL

THÈSE PRÉSENTÉE EN VUE DE L'OBTENTION

DU DIPLÔME DE PHILOSOPHIAE DOCTOR (Ph.D.)

(GÉNIE ÉLECTRIQUE)

Août 2003

*Your file Votre référence*
*ISBN: 0-612-86443-X*
*Our file Notre référence*
*ISBN: 0-612-86443-X*

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Cette thèse intitulée

CIRCUIT TECHNIQUES FOR LOW-VOLTAGE DEEP SUBMICRON CMOS ANALOG-TO-DIGITAL CONVERTERS

présentée par: FAYOMI Christian Jésus Bayodé
en vue de l'obtention du diplôme de Philosophiae Doctor
a été dûment acceptée par le jury d'examen constitué de:

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M. BRAULT Jean-Jules, Ph.D., membre

M. ISMAIL Elnaggar Mohammed, Ph.D., membre externe

*To my future Wife,*

*To my father and mother,*

*To my brothers and sisters,*

*To my dearest friends*

# *ACKNOWLEDGEMENTS*

It has been a real privilege being a graduate student in the Electrical Engineering department at "École Polytechnique de Montréal" working in close relationship with the MACS lab of McGill University. This experience gave me great opportunities to learn from engineering faculties of two universities having wide and deep expertise in engineering. I would like to directly thank people of these two universities who were particularly instrumental in contributing to my experience.

I would like to first thank my advisor, Professor Mohamad SAWAN, for his invaluable guidance throughout my long journey as a graduate student. His many years of circuit design experience have allowed me to focus on the critical and interesting issues of all the problems encountered. It has been a unique privilege to be in his group.

I would also like to express my gratitude to my co-advisor, Professor Gordon W. ROBERTS, not only for his guidance, energy and enthusiasm but also for his patience (he is the only person who knows the real meaning of this word), and for the freedom he has granted me throughout my years of study. The results of this research would not have been of the same quality without him pushing the design goals and test strategies always higher and higher.

I would like to thank the members of my thesis committee for their valuable feedback and contributions. I would like to thank Professor Yvon SAVARIA for his

insightful comments and discussions on the reliability issues of CMOS technology. Professor Jean-Jules BRAULT was a valuable member of my qualifying examination committee. I would like to thank him for giving me the opportunity to study the extension of this work application to neural network implementation in digital technology. Thanks to Professor Mohammed ISMAIL of Ohio State University for accepting to be the external reviewer of my thesis. My warmest thanks also go to Professor Ed van Tuijl of Twente University/Philips Research Laboratories Eindhoven (Netherlands) for reading my thesis and for his comments and suggestions. I would also like to thank Professor Daniel MASSICOTTE of "Université du Québec à Trois-Rivières", member of my qualifying examination committee, for his insightful comments on signal processing for communications systems and measurements.

I would like to thank my family for being very supportive and patiently listening to me trying to explain my research topic on the phone. I would like to thank my brothers and sisters Abel, Jean, Elizabeth, Cécile, and Lydia for believing in me. I could not forget my sister-in-law Ilona for always being there and feeding me when I was too tired to cook.

My sometimes flickering faith in God and in myself have remained constantly high enough to carry this work to the end. My wakefulness has become my dream and my dreams my reality. Now love is my altar, humility my strength.

I am specially thankful to Monique CHARRON LECLAIR and Gervais LECLAIR for believing me every time I said I was graduating "next year". Thanks for

their unconditional support and also for always being there and providing me with vacations that were so important and fun breaks from my work. I am very honored to be part of their family. Thanks to Lise CHARRON for reading the whole manuscript and also for her much appreciated comments and suggestions. Thanks also to Monique CARMEL for the french translation of the abstract.

I am also grateful to Gordon W. HARLING, founder of Goal Semiconductor Inc, and Marcel LAPOINTE who gave me the opportunity to design my first successive approximation analog-to-digital converter IC as first assignment as IC design engineer and thus opening a new era in my life.

Specials thanks to Micheline D. SAMSON, Vivian DUBREUIL, Marie-Josée MALETTE, Nathalie CHAGNON, Clarence K. MESSIE, Nathalie LE ROC'H, Carine LEMASSON, Isabelle LAPORTE, Maurice DUVAL and his family, Philomène R. FAYE, Nourr-Eddine RADI, Jacques SAMSON, Cécile ARSENAULT, Blandine LECLAIR, Normand LECLAIR, Damien LECLAIR, Claude CHARRON, Oury BA, Wassala NIMAGA, Ghyslain N., Pierre MARKON and his family, Jules GAUTHIER and his family, Édouard KOUASSI and his family, Françoi ABIOLA and his family, Yves ALAVO and his family, Pascal NSAME and his family, Saba HANNA and his family, Steve STRATZ from ASIC North in Burlington (Vermont), Pierre HOUDAGBA and his family, Michel HOUENAGNON, Dorothée M., Alexandra PASSARO, Gratien L., Dominique T., Magdalina DIMITROVA, Patrick B., Mike P., Martin R., Geoffrey A, Normand G., for the support they freely provided during my long path as a student.

Thanks to John OLESZKIEWICZ from IBM Microelectronics Division at Essex Junction (VT) for the opportunity to design various kinds of analog-to-digital converters. Thanks also to my co-workers on high-speed pipelined ADC project, Christopher R., Chris S., and John B with Kai D. F. on SPMC project. I will not forget my friend, Joanne HELOUVRY, at Enoch Pratt Free Library of Baltimore (MD) for providing free hardcopy of technical papers and thus giving me the time to focus on other issues.

I would also like to thank my salsa dance partners and companions Marie-Josée M., Élise D., Nicolas St-O., Julie D., Solange B., Claude L., Dominique C., Giovanna Di G., Daniel B., Alexandre L., Christine L., Luce B., Carine T., Géneviève M., and France I. to just name a few who contributed in removing some stress from my student life.

Thanks to my outdoor activity friends Josephine, Jenica, Dorothée, Nadine, Bobby, Louis-André, Marie-Josée L., Nicolas, Capucine, Patrick, Isabelle, Christine R, Verena Jr. to just name a few for giving me the chance to explore additional dimensions of my life. Special thanks to Marie-Josée MALETTE, my hike partner on the "knife-edge trail", the first person to discover my fear of huge mountains besides all the appearance and who gave me the confidence to continue.

Graduate students really spend more hours than they would like in the lab. However, the people who were there with me helped making it a more interesting experience. It has been very helpful to have fellow students who were immediately accessible and who freely gave me their support when I had technical questions. I probably learned in the lab as much as I did in the classroom. I would like to thank many students of

MACS lab such as Mohamed H., Mona S.-H., Nazmy D. A., Mourad O., Sébastien L., Geoffrey D. and many others that eluded me. Thanks to PolyStim and GRM fellow students, technicians and support specialists Jieyan Z., Abdel D., Yamu H., Moncef D., Jean-Luc T., Annie T., Saeid H., Jonathan C., Jean-François G., Claudine O., Alexander V., Réjean L. and Ghyslaine É.-C. for their support. Each of them have contributed to different areas of this expertise by sharing their work and knowledge as well as providing me valuable feedback based on the application of parts of my research to some of their own work.

Lastly, but not the least, I would like to thank the Canadian Microelectronic Corporation for fabricating the test chips, Micronet, NSERC and NATEQ for their financial support.

To All of You, thank you so much for all the support you have given me during this research. You can't believe how much I appreciate it. Find through the above lines the expression of my heart and gratitude for all you have done for me.

# *RÉSUMÉ*

*"Pour compléter la science, il faut que la pensée parcoure, d'un mouvement non interrompu et suivi, tous les objets qui appartiennent au but qu'il veut atteindre, et qu'ensuite elle le résume dans une énumération méthodique et suffisante."*
*- Réné DESCARTES, Régles pour la direction de l'esprit*

À mesure que la taille minimale du transistor des technologies CMOS diminue, la tension dans les oxydes de grille augmente au point de dépasser les limites permises dans le matériau. Les oxydes de grille nécessitent des tensions d'alimentation faibles afin d'éviter le claquage ou le quasi-claquage et du coup permettent de réduire la dissipation d'énergie dans le système.

L'obligation de réduire la tension complique de nos jours le processus de conception parce que les composants actifs se trouvent à fonctionner en dessous de leur seuil, ce qui a pour effet d'accroître les courants de fuite. Une solution consiste à utiliser une approche de polarisation dynamique du substrat qui, par la même occasion, devient un élément actif. Le concepteur doit toutefois doter le substrat d'un mécanisme de polarisation dépendant du niveau de signal à traiter. La seconde solution, qui consiste à réduire la tension d'alimentation des circuits, requiert une innovation tant au niveau de l'architecture qu'au niveau de la topologie afin d'assurer une certaine gamme dynamique quelle qu'elle soit.

Les convertisseurs analogique-numériques sont des composants essentiels assurant la communication entre les signaux analogiques externes et la puce électronique numérique. Ils ne doivent pas nuire à la précision même si le matériel dans lequel ils sont intégrés se compose de dispositifs très imparfaits. Voilà pourquoi les convertisseurs justifient toutes les connaissances acquises au cours des vingt dernières années en matière de conception, destinées à contourner les contraintes et les défaillances inhérentes aux circuits intégrés.

La présente thèse vise à étudier la faisabilité des techniques de conception de circuits microélectroniques fiables destinés aux convertisseurs opérant à bas voltage dans les procédés CMOS submicroniques standards et à développer celles-ci. Nous avons étudié les contraintes de tension inhérentes aux technologies CMOS submicroniques puis examiné la manière d'optimiser l'utilisation des transistors MOS afin de concevoir des circuits analogiques fiables. L'accent a été mis sur des solutions matérielles qui n'exigent aucune modification du procédé. Les contributions scientifiques suivantes découlent de notre travail:

- Une nouvelle méthode de conception du comparateur analogique différentiel à verrou (*latch*)en CMOS destiné aux applications à basse tension. Cette méthode repose sur l'étage d'entrée de type rail à rail à transconductance constante.
- Une nouvelle méthode de conception des échantillonneurs-bloqueurs. Cette conception repose sur une nouvelle approche d'intégration de l'interrupteur (*switch*) CMOS analogique à tension doublée. Une nouvelle façon de doubler la

tension d'horloge a aussi été proposée. L'interrupteur redondant a été utilisé afin de réduire l'injection de charge induite par l'interrupteur CMOS, ce qui a pour effet d'améliorer la précision de l'échantillonnage.

- Une stratégie de conception d'amplificateur opérationnel de type rail à rail afin de maximiser la gamme dynamique d'entrée/sortie. Le circuit utilise une nouvelle technique de décalage de niveau du signal d'entrée et un étage d'entrée de classe AB. L'étage de sortie utilise la technique de polarisation dynamique basée sur des circuits à condensateurs commutés.

Ces blocs analogiques ont permis de concevoir deux architectures de convertisseurs analogique-numériques à approximations successives dans la technologie submicronique CMOS standard de 0.18 µm. La résolution de ces convertisseurs opérant à une tension d'alimentation de 1 V est de 10 bits avec une fréquence de conversion de 200 K-échantillons par seconde.

Les contributions originales de cette thèse par articles ont fait l'objet d'un premier article de journal accepté pour publication dans la revue *Kluwer Academic Publishers Analog Integrated Circuits and Signal Processing*. Le second article est présentement à l'étude afin d'être publié dans la revue *IEEE Transactions on Circuits and Systems II*.

# *ABSTRACT*

*"The greater becomes the volume of our sphere of knowledge, the greater also becomes its surface of contact with the unknown."*

*- Jules SAGRET*

As the devices scale to smaller dimensions, the voltage fields in the oxides grow to exceed the safe operating limits of the materials. The thinner oxides require reduction in the operating voltages to minimize field-induced oxide breakdown, while creating the "free" benefit of reducing the operating power.

This lower voltage complicates the design process. An issue with lower voltages is that the active devices may be operating at a subthreshold level, increasing leakage currents. One solution is to move to an active substrate biasing scheme, which means that substrates also become an active circuit element. The designer must add some function to the bulk biasing as a function of the absence or presence of the signals. Lower operating voltages require new architectures and circuit topologies to enable any dynamic range.

Data converters are essential parts that enable communication between the external analog world and the digital silicon chip. They should not compromise precision even though the hardware in which they are implemented relies on semiconductor devices known for their poor accuracy. Therefore, converters capitalize on design expertise

accumulated during the last 20 years to circumvent the limitations and impairments inherent to integrated circuits.

The objective of this thesis is to investigate the feasibility of reliable data converters design techniques in standard CMOS processes for low-voltage operation. We examine the voltage limitations of CMOS technology and how analog circuits can maximize the utility of MOS devices without degrading reliability. Emphasis is placed on circuit solutions that do not require process enhancements. The specific research contributions of this work consist of:

- A new approach to the design of a CMOS differential latched comparator suitable for low voltage applications. The novel approach makes use of the well-known constant-gm rail-to-rail input stage used in amplifiers.
- A sample-and-hold circuit based on a novel implementation of the bootstrapped low-voltage analog CMOS switch. The heart of this circuit is a new low-voltage and low-stress CMOS clock voltage signal booster. Through the use of a dummy switch, the charge injection induced by the bootstrapped switch is greatly reduced resulting in improved sample-and-hold accuracy.
- A design strategy for a rail-to-rail input / output operational amplifier. The circuit makes use of a novel level shifting technique of the input signal and a dynamically biased class AB output stage based on a switched-capacitor configuration.

Those building blocks have been used to implement two architectures for a 1-V, 10-bit 200-kS/s successive approximation analog-to-digital converter in a 0.18 μm digital CMOS process.

The original contributions and main conclusions of this manuscript-paper based thesis are the subjects of a first journal manuscript accepted for publication in *Kluwer Academic Publishers* *Analog Integrated Circuits and Signal Processing* and of a second submitted for publication in *IEEE Transactions on Circuit and Systems II*.

# *CONDENSÉ EN FRANÇAIS*

*"Pour découvrir la vérité, l'homme doit s'affrranchir de toute autorité; en lui brille la lumière qui éclaire tout homme venant en ce monde, dont les clartés peuvent seules lui faire découvrir ce qui est."*

*- Réné DESCARTES, Discours de la méthode*

La réduction d'échelle des technologies est en train d'emmener les dispositifs CMOS au point de blocage. Il n'est pas question d'arrêter les développements des technologies CMOS, mais encore une fois, on se trouve devant une nécessité incontournable d'innovation. Ce blocage apparaît aussi bien au niveau du dispositif qu'au niveau des méthodes de conception des cellules microélectroniques.

La génération 0.1 μm semble être la dernière dans la longue chaîne des technologies qui, moyennant le changement d'échelle des dimensions, de la tension d'alimentation et du niveau de dopage, assuraient les performances et les densités d'intégrations accrues. Cette chaîne ne s'arrête pas brutalement mais sans introduction de nouveaux éléments et le développement de nouvelles approches de conception des circuits microélectroniques, les performances des dispositifs au lieu de croître pourront décroître.

Cette thèse propose une solution alternative, qui permet l'utilisation de la technologie CMOS standard, c'est-à-dire facilement accessible et pas très coûteuse, pour la conception des circuits microélectroniques intégrés dédiés aux convertisseurs analogique-numériques à basse tension d'alimentation.

Dans le texte suivant, le travail effectué est expliqué brièvement en soulignant l'apport original fourni par cette thèse par articles de revue avec comité de lecture. Les références aux figures, aux équations et aux indications bibliographiques sont référées au texte en anglais.

## I. INTRODUCTION

L'augmentation de la densité d'intégration et la rapidité sans cesse croissante des circuits a conduit au développement des dispositifs microélectroniques. Chaque année, les chercheurs s'emploient à réduire la taille de ces dispositifs. L'épaisseur minimum d'oxyde de grille actuellement atteinte est de 20 Å, soit 7 couches atomiques.
L'organisation de ce document est le suivant. Dans la section II, nous aborderons les défis techniques liés à la conception de nouveaux dispositifs microélectroniques. Les approches de conception proposées seront discutées dans la section III. La section IV est exclusivement réservée aux résultats des tests expérimentaux et nous conclurons par la section V sur les applications et extensions futures du projet.

## II. LES DÉFIS TECHNIQUES DE LA MICROÉLECTRONIQUE À BAS VOLTAGE

La réalisation des capacités est souvent indépendante de l'alimentation. Cependant, une superficie ou surface plus grande serait requise avec la réduction de la dimension minimale des procédés submicroniques. Des nouvelles approches doivent donc être développées.

Le plus grand impact se fait sentir au niveau de la conception des amplificateurs opérationnels. Une des conséquences de la basse tension d'alimentation est la réduction

de la plage dynamique d'entrée comme le montre la figure 2.1. On assiste aussi à une réduction de la bande passante. Les nouvelles méthodes de conception doivent donc contribuer à maximiser la gamme dynamique du signal d'entrée tout en maximisant la bande passante [ABO99a]. Un survol détaillé des solutions adoptées a été présenté au chapitre 3. Elles consistent à utiliser le transistor MOS dans des régions d'opérations non conventionnelles difficilement modélisables au niveau des simulateurs actuels.

La conception des références de tension est aussi affectée par la réduction de l'alimentation dans les procédés submicroniques. La sortie typique d'une référence de tension est de l'ordre de 1.26 V. Elle est indépendante de la tension d'alimentation du circuit ainsi que de la température. Pour un fonctionnement optimal, ce circuit (figure 2.2) requiert une tension d'alimentation de l'ordre de 1.5 V. La conception d'une référence de tension dans un procédé submicronique alimenté à 1.0 V [SIA02] s'avère donc être un défi de taille. Une solution (au niveau circuit) doit être apportée. Certaines de ces approches ont été abordées au chapitre 3. Les approches de conception des références de tension à bas voltage d'alimentation ne font pas partie intégrante de cette thèse. Cependant les nouvelles techniques de conception des amplificateurs opérationnels proposées dans cette thèse peuvent être utilisées pour solutionner les problèmes liés aux références de tension.

La conception des portes de transmission est aussi affectée par la réduction de l'alimentation comme en témoigne la figure 2.3. Pour des tensions d'alimentation très basse (de l'ordre de 0.65 V), une plage interdite apparaît. Dans cette plage, le signal d'entrée ne passe plus à travers la porte de transmission (figure 2.3c). Les approches de

conception apportées afin de palier à cette situation consistent à doubler le signal de contrôle de la porte de transmission analogique et du coup peuvent induire d'autres problèmes tels que le claquage de l'oxyde de grille à cause de l'amincissement de cette dernière comme le montre la figure 2.4. Dans cette thèse, une solution a été apportée à ce problème.

La structure MOS constitue l'élément de base des circuits intégrés. Elle est composée d'un sandwich grille-oxyde-silicium formant une capacité dont l'électrode de grille est accessible par les contacts source et drain. L'épaisseur de l'oxyde de grille, des technologies CMOS actuelles, atteint des valeurs de quelques nanomètres et sera bientôt inférieure à 2 nm pour les générations sous 0.1 μm. L'épaisseur de l'oxyde est estimée à 1/40 de la longueur minimale du transistor permise dans le procédé [MEA94]. Cette réduction de l'épaisseur du diélectrique de grille favorise l'apparition de phénomènes physiques comme la poly-déplétion de grille ou les effets quantiques qui limitent les performances des dispositifs MOS en terme de capacité et de courant de fuite. L'effet de poly-déplétion est dû à la chute de potentiel dans l'électrode de grille non métallique et réalisée en polysilicium pour les technologies CMOS. Cette perte de potentiel dans la grille entraîne une diminution de l'efficacité du couplage capacitif grille-canal et donc du courant disponible dans le transistor. Les effets de confinement quantique des porteurs à l'interface silicium-oxyde conduisent également à une réduction de la capacité maximum en inversion de la structure MOS atténuant du coup ses performances. Les phénomènes quantiques sont également responsables de l'accroissement des courants de fuite de grille par l'effet tunnel. De plus, les structures MOS à oxydes de grille ultra

minces sont sensibles à de nouveaux mécanismes de dégradation, tels que les courants de fuite induits par le stress, le quasi-claquage et le claquage qui pourraient réduire leur durée de vie. Ces mécanismes de dégradation des oxydes sont d'autant plus critiques que leurs taux de génération sont exponentiellement accélérés par le champ électrique supporté par la structure comme le montre l'équation (2.12). Divers autres phénomènes tels que le «*drain induced barrier*», « *lowering*, *punch-through*», existent dans les procédés submicroniques pour ne citer que ceux-là. Les équations (2.14) à (2.16) les décrivent de façon quantitative.

Les approches de conception de circuits électroniques en technologie submicronique doivent donc tenir compte de ces phénomènes. La section ci-dessous décrit les méthodes de conception proposées. L'emphase a été mise sur la fiabilité à long-terme.

## III. CIRCUITS INTÉGRÉS DÉDIÉS À DES APPLICATIONS À BAS VOLTAGE

Dans le souci constant de répondre aux défis liés à la conception de circuits intégrés, introduits par les nouvelles technologies CMOS submicroniques, des approches de conception fiables ont été proposées dans cette thèse. L'accent a été mis sur les modules couramment utilisés dans la conception des convertisseurs analogique-numériques. Il s'agit entre autres de comparateurs analogiques, d'amplificateurs opérationnels, d'échantillonneur-bloqueurs puis de convertisseurs numérique-analogiques.

Le premier circuit proposé est un comparateur analogique à large gamme dynamique d'entrée, destiné à opérer à une tension d'alimentation de 1.65 V. Le fruit de

ce travail a été publié dans le compte rendu d'une conférence avec comité de lectures [FAY00a]. Le diagramme bloc du circuit est montré à la figure 5.6 et est constitué du circuit de polarisation, d'un étage d'entrée de type rail à rail et d'un bistable (*latch*). Les détails techniques de ces différents éléments constitutifs sont montrés aux figures 5.7 à 5.9. Les facteurs limitant la performance de ce circuit sont les tensions de décalage (*offset*) liées à l'étage rail à rail et au bistable. L'effet de décalage dû au latch est atténué par le gain de l'étage différentiel d'entrée. L'optimisation de cet étage permet de maximiser la performance sur cet aspect.

Une autre architecture de comparateur analogique à large gamme dynamique et pouvant opérer jusqu'à 0.65 V a été proposée telle qu'elle est montrée à la figure 5.10. Ce comparateur fut utilisé dans la conception d'un convertisseur analogique-numérique [FAY01b].

Un autre élément essentiel à la conception des convertisseurs analogique-numériques est l'interrupteur MOS (*switch*) souvent utilisé comme échantillonneur-bloqueur. Pour que cet interrupteur soit capable de transmettre tous les signaux entre la tension d'alimentation et la masse, il faut qu'il soit composé de deux transistors (un canal n et un canal p) montés en parallèle comme le montre la figure 4.1c. Un des problèmes liés au *scaling* de la technologie CMOS est que la valeur absolue des tensions de seuil des transistors n'est pas réduite dans le même rapport que la tension d'alimentation. Cette réduction est approximativement proportionnelle à la racine-carrée de l'alimentation [MEA94]. Si la tension d'alimentation baisse en dessous d'une certaine valeur critique $V_{DD,crit}$, l'interrupteur n'est plus capable de transmettre les signaux analogiques dans une

certaine gamme entre 0 V et $V_{DD}$ (figure 2.3c). Pour solutionner ce problème nous avons proposé une nouvelle approche de conception simple de ce circuit. Le diagramme bloc du circuit proposé est montré à la figure 4.4 tandis que les détails techniques sont fournis aux figures 4.5 à 4.11. Un des attributs de ce circuit est la constance de sa résistance en fonction du signal d'entrée, attribut essentiel à la réduction de la distorsion. Un autre critère dont nous avons tenu compte dans la conception est l'injection de charges qui peut aussi atténuer de façon significative les performances du circuit. Le circuit proposé dans cette thèse (figure 4.6) solutionne ces problèmes. Ce circuit a été utilisé dans la conception d'un échantillonneur-bloqueur pouvant fonctionner à des tensions d'alimentation aussi basses que 0.65 V. Les résultats de ce travail ont été publiés dans un compte rendu de conférence [FAY00b]. Une autre partie de ce travail est l'objet d'un article de journal avec comité de lecture IEEE Transactions on Circuits and Systems II et est présentement sous évaluation.

Le troisième circuit proposé est un amplificateur opérationnel de type rail à rail destiné à opérer à des tensions d'alimentation de l'ordre de 1-V et moins [FAY01a]. Le diagramme bloc de ce circuit est montré à la figure 5.1. Il est constitué d'un circuit de décalage de niveau, d'une paire différentielle et d'un étage de sortie de classe AB. Le circuit de décalage de niveau (figure 5.2) permet de convertir un signal analogique compris entre 0 V et $V_{DD}$ en un signal situé entre $-V_{DD}$ et 0 V. Ce signal est suffisant pour activer les transistors pMOS de la paire différentielle d'entrée (figure 5.3). De plus il permet de faire fonctionner tous les transistors en inversion forte (*strong inversion*). L'étage de sortie de type AB (figure 5.4) permet d'avoir une large gamme dynamique de

sortie. D'autres solutions alternatives de conception du circuit de décalage de niveau et de la paire différentielle d'entrée sont proposées à la figure 5.5. La caractéristique intéressante de ce circuit est la large gamme dynamique d'entrée/sortie.

Un quatrième circuit plus complexe a été aussi proposé dans cette thèse. Il s'agit d'un convertisseur analogique-numérique de type rail à rail [FAY01b]. Ce circuit fait usage de certains des éléments décrits ci-dessus et son diagramme bloc est montré à la figure 5.13. Une analyse détaillée du choix des composants a été aussi abordée. Diverses solutions alternatives de conception ont été discutées.

La prochaine section porte sur les tests expérimentaux effectués pour vérifier la faisabilité des concepts abordées ci-dessus.

## IV TESTS EXPÉRIMENTAUX ET SIMULATION

Après avoir démontré la faisabilité de circuits microélectroniques dans les technologies submicroniques à bas voltage, nous avons validé les concepts au niveau expérimental. Tous les circuits ont été implémentés dans la technologie 0.18 µm de TSMC. Il s'agit d'un procédé dédié aux circuits numériques. Il dispose d'un procédé à substrat de type p d'un puits (*well*) de type n disposant d'une seule couche de polysilicium. Les seuils typiques des transistors de type N et P sont de 0.5 V et –0.6 V respectivement.

Les simulations ont été effectuées en utilisant le logiciel Hspice.

Au niveau test, les générateurs de signaux utilisés sont de type Hewlett Packard modèles HP81130A et HP33120A. Les signaux de sortie ont été visualisés avec les oscilloscopes de type Tektronix TDS320 et TDS7154.

Le circuit de l'échantillonneur-bloqueur (figure 4.6) a été testé afin de vérifier la constance de la résistance, la linéarité de l'erreur dynamique induite et le niveau de distorsion.

Nous avons mesuré la résistance de l'interrupteur (figure 4.6) en utilisant la configuration montrée à la figure 6.3. Les résultats obtenus (figures 6.4 à 6.6) confirment la constance de la résistance en fonction du signal d'entrée. La figure 6.7 montre la linéarité de la conductance moyenne de l'interrupteur en fonction de la tension d'alimentation. Ces résultats sont en conformité avec les modèles théoriques développés (relation 4.5) aux erreurs expérimentales près. Un test purement fonctionnel a été effectué afin de valider le concept échantillonnage-blocage. Le schéma de principe de la figure 6.9 a été utilisé à cette fin. Le test fonctionnel fût effectué pour les tensions d'alimentation de 0.65 et 1 V et les résultats obtenus sont montrés aux figures 6.12 à 6.13 respectivement pour une fréquence d'horloge (échantillonnage) de 250 KHz. L'erreur dynamique (injection de charge et *clock feedthrough*) induite dans l'échantillonneur-bloqueur varie linéairement en fonction du signal d'entrée comme le montre la figure 6.11. Le niveau de distorsion a été testé en utilisant le concept de l'échantillonnage cohérent [ROB95], [BUR01], [GRO97]. Une fenêtre constituée de 256 échantillons a été utilisée à cette fin. Les tests ont été effectués pour deux fréquences d'horloges (0.25 et 1 MHz) et pour des tensions d'alimentation de 0.65 et 1 V. Le signal de sortie a été prélevé et une analyse spectrale fût effectuée en utilisant Matlab. Les résultats de ces analyses sont montrés aux figures 6.14 à 6.17. Le rapport signal sur bruit est de l'ordre de 71.05 dB et 45.78 dB pour des tensions d'alimentation respectives de 1 V et 0.65 V sous une fréquence d'horloge de

0.25 MHz. Ces valeurs correspondent à une précision de 11.5 bits et 7.3 bits respectivement. Ces résultats sont excellents comparés aux circuits complexes utilisés à une tension d'alimentation de 3.3 V afin d'assurer le même niveau de performance [KOB01], [SUZ02], [WAL99].

Des simulations ont été effectuées sur les autres circuits proposés. La constance de la transconductance de l'étage d'entrée différentielle du comparateur analogique (figure 4.25) a été démontrée. Les performances fonctionnelles dynamiques ont été également validées. Les résultats sont montrés aux figures 6.18, 6.19 et au tableau 6.1. Les temps de montée, de descente et les délais de propagation sont quasi-constants et presque indépendants du mode commun.

La gamme dynamique d'entrée/sortie de l'amplificateur opérationnel (figure 4.20) a été simulée au niveau logiciel ainsi que sa réponse en fréquence et au signal impulsionnel. Les résultats sont montrés aux figures 6.20 à 6.23. Le circuit possède une large bande dynamique d'entrée/sortie de presque 1 V. La bande passante du signal est de l'ordre de 26.6 MHz avec une marge de phase de 67 degrés sous une charge résistive et capacitive de 5pF et 20 kΩ. L'amplificateur opérationnel dissipe une puissance de 400 μW.

La simulation fonctionnelle du convertisseur analogique-numérique (figure 5.4) prouve que le circuit peut opérer à 1 V sous une fréquence d'échantillonnage de 200 K échantillons/secondes. La gamme du signal d'entrée peut aller de 0 à 1 V. Il est à noter que la fréquence d'échantillonnage choisie est intimement liée à la précision de l'échantillonneur-bloqueur. Ce dernier présente une résolution de l'ordre de 11.5 bits

sous une fréquence de 0.25 MHz comme le témoigne la figure 6.14. Une résolution de plus de 10 bits est difficilement réalisable avec ce type de configuration de convertisseurs. Cette limitation est due à la structure résistive du circuit de convertisseur numérique-analogique.

Pour résumer, les circuits proposés correspondent bien aux attentes des modèles théoriques développées. Les prochains paragraphes résument la performance et les futures orientations du projet.

## V. CONCLUSION ET RECOMMANDATIONS

L'idée à la base de cette thèse est le développement des approches de conception de circuits microélectroniques dédiés aux convertisseurs analogique-numériques à bas voltage d'alimentation dans les technologies submicroniques. Pour cette raison nous avons étudié les problèmes liés aux technologies submicroniques standard. Cette étude nous a amené à développer des approches qui permettent de concevoir des circuits intégrés fiables et fonctionnels dans ces technologies. Les performances des circuits proposés ont été validées tant au niveau matériel qu'au niveau logiciel.

Une bonne continuation de ce projet serait de faire des tests de fiabilité à long terme sur les modules matériels développés. Le simulateur de fiabilité *Berkeley Reliability Tool* [HU92] peut être utilisé.

Les structures microélectroniques complètement différentielles présentent une bonne immunité au bruit. Une autre continuation de projet sera la modification des topologies proposées afin d'en faire des structures complètement différentielles. Finalement

des tests expérimentaux au niveau matériel doivent être effectués afin de valider les modifications.

Une validation au niveau matériel de la technique de conversion analogique-numérique à approximation successive proposée au chapitre 5 constitue également une bonne continuité du projet. Des tests intensifs des linéarités différentielle et intégrale ainsi que les mesures du gain et de la distorsion doivent être effectués. L'utilisation des circuits proposés dans la conception de convertisseurs analogique-numériques de type pipeline et à sur-échantillonnage, pour ne citer que ceux-là, serait souhaitable.

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# *LIST OF ABBREVIATIONS*

| | |
|---|---|
| A/D | Analog-to-Digital |
| ADC | Analog-to-Digital Converter |
| BGR | BandGap Reference Voltage |
| BiCMOS | Bipolar CMOS |
| BJT | Bipolar Junction Transistor |
| CM | Common Mode |
| CMFB | Common Mode Feedback |
| CMOS | Complementary Metal Oxyde Semiconductor |
| CMR | Common Mode Range |
| D/A | Digital-to-Analog |
| DAC | Digital-to-Analog Converter |
| dB | Decibel |
| DC | Direct Current |
| DFT | Discrete Fourier Transform |
| DIBL | Drain Induced Barrier Lowering |
| DLL | Delay Locked Loop |
| DNL | Differential Non-Linearity |
| DR | Dynamic Range; |
| DSP | Digital Signal Processing |
| ENOB | Effective Number Of Bits |

| | |
|---|---|
| FFT | Fast Fourier Transform |
| GBW | Gain-Bandwidth product |
| GIDL | Gate Induced Drain Leakage |
| HCI | Hot Carrier Induced |
| IC | Integrated Circuit |
| INL | Integral Non-Linearity |
| ITRS | International Technology Roadmap for Semiconductors |
| LDD | Lightly Doped Drain |
| LSB | Least Significant Bit |
| MDAC | Multiplying Digital-to-Analog Converter |
| MOS | Metal Oxide Semiconductor |
| MOSFET | Metal Oxide Semiconductor Field Effect Transistor |
| MOST | MOS Transistor |
| MSB | Most Significant Bit |
| nMOS | n-channel Metal Oxide Semiconductor |
| NPN | n-type Bipolar Transistor |
| OTA | Operational Transconductance Amplifier |
| Opamp | Operational Amplifier |
| PLL | Phase Locked Loop |
| PNP | P-type Bipolar Transistor |
| pMOS | p-channel Metal Oxide Semiconductor |
| PSD | Power Spectral Density |

| | |
|---|---|
| PSRR | Power Supply Rejection Ratio |
| PTAT | Proportional To Absolute Temperature |
| RMS | Root Mean Square |
| SIA | Semiconductor Industry Association |
| S/H | Sample-and-Hold |
| SC | Switched Capacitor |
| SNDR | Signal-to-Noise-and-Distortion Ratio |
| SFDR | Spurious Free Dynamic Range |
| SNR | Signal-to-Noise Ratio |
| SO | Switched Opamp |
| SoC | System on a Chip |
| TDDB | Time Dependent Dielectric Breakdown |
| T/H | Track-and-Hold |
| THD | Total Harmonic Distortion |
| VCO | Voltage Controlled Oscillator |
| VHDL | Very High Speed Integrated Circuits Hardware Description Language |
| VLSI | Very Large Scale Integration |
| VSDM | Very Deep Submicron |

# *LIST OF SYMBOLS*

| | |
|---|---|
| $\mu$ | Carrier mobility |
| $\gamma$ | Body effect constant of MOSFET |
| $\lambda$ | Output impedance constant of MOSFET |
| $\sigma^2$ | Variance |
| A | Open-loop DC gain |
| $A_{Vth}$ | Threshold voltage matching parameter |
| $C_G$ | Gate capacitance |
| $C_L$ | Load capacitance |
| $C_{ox}$ | Capacitance per unit area |
| f | Frequency |
| $f_S$ | Sampling frequency |
| $g_m$ | Gate small-signal transconductance |
| $g_{ds}$ | Source drain small-signal conductance |
| $I_D$ | Drain current |
| $I_{DS}$ | Drain-to-source current (channel current) |
| k | Boltzmann's constant |
| L | Channel length |
| $L_{min}$ | Minimum channel length |
| n | Number of bits |

| | |
|---|---|
| $N$ | Number of bits |
| $q$ | Electron charge |
| $R_L$ | Load resistance |
| $R_{ON}$ | Switch ON-resistance |
| $T$ | Absolute Temperature, sampling period |
| $t$ | Time |
| $t_{ox}$ | Oxide thickness |
| $V_A$ | Characteristic voltage in first order channel length modulation |
| $V_B$ | Body or bulk voltage |
| $V_D$ | Drain voltage |
| $V_{DD}$ | Positive supply voltage for digital circuit |
| $V_{DDA}$ | Positive supply voltage for analog circuit |
| $V_{DS}$ | Drain-source voltage |
| $V_{DS,\,sat}$ | Drain-source saturation voltage |
| $V_{eff}$ | Effective voltage of MOSFET |
| $V_{FS}$ | Full scale voltage |
| $V_G$ | Gate voltage |
| $V_g$ | Gate voltage |
| $V_{GS}$ | Gate-source voltage |
| $V_{off}$ | DC offset voltage |
| $V_{ref}$ | Reference voltage |
| $V_S$ | Source voltage |

| | |
|---|---|
| $V_{SB}$ | Source body (bulk) voltage |
| $V_{SS}$ | Negative supply voltage for digital circuit |
| $V_{SSA}$ | Negative supply voltage for analog circuit |
| $V_{th}$ | Threshold voltage |
| $V_T$ | Thermal Voltage |
| W | Channel width |
| x | Distance along the channel |

# *Chapter 1*

# *INTRODUCTION*

*"Every great advance in science has issue from a new audacity ... of the imagination."*

*- John Dewey*

## 1.1 Motivation

Down-scaling of CMOS device dimensions has been the major stimulation for the continuing growth of the microelectronics industry over the past three decades. This trend of steady down-scaling was first formulated by Gordon E. Moore and is better known as Moore's law [MOO65]. In 1965 G. Moore, R&D director at Fairchild Semiconductor, today chairman emeritus of Intel Corporation, published a semi-log plot of the number of components on a silicon chip versus the date of first availability. The result was a straight line representing almost a doubling per year. In the later years, the rate relaxed somewhat to a doubling every 18 months. This is still the rate today and is expected to prevail for some time.

Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs) have been around quite some time now. The success of these silicon-based devices is due, apart from the possibility to reduce their dimensions down to almost nanometer scale dimensions, to the stable high quality silicon-silicon dioxide interface and to the ability

to interconnect millions to billions of devices on a single chip to form an integrated circuit. The basic concept of the MOSFET and its operation was formulated almost seventy years ago [LIL30], even before the experimental discovery of the bipolar junction transistor by J. Bardeen, W. H. Brattain and Shockley [BAR48], [SHO49]. However, it was not until 1960 that the first silicon MOSFET was built by Kahng and Attalla [KAH60]. Ironically enough, the main reason for the rather late realization of a functioning MOSFET was the difficulty to realize a high quality interface between a dielectric layer and a semiconductor, a requirement for proper MOSFET action. Today, after many generations of down-scaling of CMOS devices, the gate oxide thickness is approaching atomic dimensions and we are close to fundamental limits imposed by quantum mechanisms. Also, the reliability of the gate-oxide is becoming a major concern. If the scaling trend continues as predicted by the International Technology Roadmap for Semiconductors [SIA02], $SiO_2$ may not be able to meet the future reliability requirements under normal operating conditions [STA98].

In recent years, much attention has been paid to the reduction of the supply voltage and the power consumption of mixed-signal CMOS integrated circuits and systems. In addition to down scaling, this is primarily due to the increasing importance of battery-powered electronic. In fact, three main reasons can be given for the advent of low-voltage circuits:

- As the channel length is scaled down into submicron and the gate oxide thickness becomes only several nanometers, the supply voltage has to be

reduced in order to ensure device reliability (down to 1.5 V and below in the near future) [SIA02].

- The second reason emanates from the increasing number of components on a single chip. A silicon chip can only dissipate a limited amount of power per unit area. Since the increasing density of components allows more electronic functions per unit area, the power per electronic function has to be lowered in order to prevent overheating of the chip.
- The third reason is dictated by portable, battery-powered equipment. In order to have an acceptable operation period from a battery, both the power and the supply voltage have to be reduced considering the slow progress in developing high capacity batteries.

A particular consequence of the lowered power supply is the need for rail-to-rail input stages in most current building blocks in order to compensate for the reduced input common-mode and dynamic range. The power dissipated by analog circuitry, however, does not necessarily decrease when the supply voltage lowers, as the traditional stacking of transistors has to be replaced by cascaded folding techniques, which inevitably increase the current drawn from the supply. Hence, to decrease the power dissipated in low-voltage analog circuits, the design has to be kept smaller and as simple as possible.

The new smaller size process technologies also offers opportunities to operate at high frequencies while consuming less power. This fact applies partially to analog circuits since additional current is often needed to keep the same performance when the power supply voltage is decreased.

Another important design aspect is the transistor region of operation. For instance, with transistors operating in strong inversion, more power (than the minimum required) is often used to meet the specifications. Optimal design involves minimum power consumption and/or silicon area while meeting performance requirements. Designers should also explore design using transistors operating in non-conventional ways. The extreme cases of weak and strong inversions do not provide, in most case, a good tradeoff between frequency response, power consumption and silicon area. Thus, we should consider a one-equation transistor model for all regions [SAN99], [CUN98], which would allow designers to optimize the circuit performance at minimum cost. Bulk-driven and floating-gate techniques which can help to produce efficient low-voltage circuits with reduced power supply restrictions, have been extensively discussed in [YAN00]. In this chapter, research objectives and methodologies are addressed in Section 1.2, while Section 1.3 presents a summary of the key contributions and of the thesis organization.

## 1.2 Research objectives and methodologies

The main objective of this thesis is to investigate the feasibility of reliable data converters design techniques in standard CMOS processes for low-voltage operation. We will propose circuit techniques and design methods for low-voltage analog building blocks such as sample-and-hold, opamp, comparator, etc. Those building blocks will be used to implement a complete successive approximation ADC.

The following systematic work methodology will be used to attain the main objective.

- Overview of past and current research status to cover the existing design techniques for low-voltage circuits;
- Investigation of the limitations imposed by the restriction of low supply voltage;
- Study of the reliability issues involved in deep submicron CMOS circuit design;
- Development of circuit techniques for low-voltage deep submicron building blocks used in the design of data converters (sample-and-hold, opamp, comparator, D flip-flop, digital-to-analog converters);
- Application of completed building blocks to design a 1-V successive approximation ADC in a 0.18 μm standard digital CMOS process;
- Results, synthesis and discussions with further development.

## 1.3 Research contributions and organization of the thesis

The contributions presented in this thesis have been partially reported in several conference and journal and summarized below.

- We present in [FAY03a] an overview of circuit techniques used to design reliable low-voltage (1-V and below) analog building blocks in deep submicron standard CMOS processes. The challenges of designing such low-voltage and reliable analog circuits are addressed both at electronic circuit and physical layout levels. State-of-the-art circuit topologies and techniques (input level shifting, bulk and current driven, DTMOS), used to build main analog modules (operational

amplifier, analog CMOS switches) are covered with the implementation of MOS capacitors.

- In [FAY00a], we proposed a new approach to the design of a CMOS differential latched comparator suitable for low voltage applications. The novel approach makes use of the well-known constant-gm rail-to-rail input stage used in amplifiers. The circuit consists of a constant-gm rail-to-rail common-mode OTA (compared to previous work [CHU99], [HES91], [KUM86] and [SHI91]) followed by a regenerative latch. The circuit dissipates less than 86 μA with a supply voltage of 1.65 V in a standard CMOS 0.18 μm digital process. At the heart of the design is a track-and-latch circuit. This circuit reduces the number of gain stages normally required in an asynchronous or multi-stage comparator [JOH97], thereby reducing the power and silicon area requirements, as well as decreasing the comparator settling time. The net result is a more power efficient comparator.
- We proposed in [FAY00b] a sample-and-hold circuit based on a novel implementation of the bootstrapped low-voltage analog CMOS switch. Also, corresponding experimental results were reported in [FAY03b]. The heart of this circuit is a new low-voltage and low-stress CMOS clock voltage signal booster. Through the use of a dummy switch, the charge injection induced by the bootstrapped switch is greatly reduced resulting in improved sample-and-hold accuracy. The circuit has been implemented in a standard CMOS 0.18 μm digital process. The experimental results show that operation is possible for supply voltages close to transistor threshold (0.6 V).

- In [FAY01a], our focus was the design strategy for a rail-to-rail input/output operational amplifier. The circuit relies on a novel level shifting technique of the input signal and a dynamically biased class AB output stage based on a switched-capacitor configuration. The power supply of the amplifier is as low as 1-V while providing a 26.6 MHz unity gain frequency and a 67-degree phase margin with a load condition of 5 pF and 20 kΩ. The overall circuit dissipates 400 μW.
- Finally, we presented in [FAY01b] two architectures for a 1-V, 10-bit 200-kS/s successive approximation analog-to-digital converter. The 10-bit ADC designed for medium resolution applications, is based on a novel track-and-hold circuit implemented with a bootstrapped low-voltage analog CMOS switch. We also introduced a novel rail-to-rail track-and-latch comparator circuit. A pMOS-only ladder containing a rail-to-rail current-to-voltage converter, performs the DAC function in the second ADC topology whereas a conventional R-2R ladder is used in the first one.

The organization of this journal papers based thesis is briefly described below.

We addressed in Chapter 2, challenges and issues in low voltage deep submicron CMOS analog design, with the main limitations imposed by the reduction in circuit supply voltage. Concerns with reliability in deep submicron design are also reviewed.

We surveyed in Chapter 3 the state-of-the-art circuits (opamps, bandgap, comparators, switches), suitable for low-voltage deep submicron analog design in standard CMOS process. The implementation of CMOS-based capacitor is also

addressed. This chapter is the subject of a journal manuscript accepted for publication in the *Kluwer Academic Publishers* journal Analog Integrated Circuits and Signal Processing.

Chapter 4 covers the reliable implementation strategy for low-voltage analog CMOS switch used as a sample-and-hold circuit. It contains another journal paper, submitted for publication in the *IEEE Transactions on Circuit and Systems II*. The main focus of this paper is the design strategy for low-voltage analog CMOS switches. The heart of this switch is a novel switched-capacitor based voltage doubler.

Finally, in Chapter 5, we proposed a 1-V operational amplifier with rail-to-rail input/output. We, also, introduced various design strategies for rail-to-rail CMOS comparators along with the design procedure for a 1-V and 10-bit successive approximations ADC.

Detailed results are presented in Chapter 6 and we conclude in Chapter 7 with main contribution's summary and recommendations to suggest a future development of this work.

# *Chapter 2*

# *CHALLENGES IN DEEP SUBMICRON LOW-VOLTAGE CMOS CIRCUITS*

*"No pessimist ever discovered the secrets of the stars ... or sealed to an unchartered land ...or opened a new heaven to the human spirit."*

*- Helen Keller*

The evolution in CMOS processes aims at increasing the performance of digital systems. To increase their performance (speed) while reducing their cost (power consumption and area), the minimum transistor dimensions and the supply voltage steadily decrease with newer CMOS processes [SIA02]. However, most chips are not purely digital systems, but are, to some extent, mixed-signal systems. Besides a typically large digital core, there are analog building blocks including phase-lock-loops, power-on-resets, analog-to-digital converters (ADCs), filters, opamps, to name just a few. The performance of these analog blocks does not necessarily improve with newer CMOS generations [ANN99a]. In this chapter, the effects of CMOS technology and supply voltage on the most commonly used analog blocks will be analyzed and reliability issues will be addressed.

## 2.1 Low-voltage CMOS analog circuit design issues

### *2.1.1 Capacitors*

The implementation of poly-poly capacitors is not affected by the reduction of the supply voltage level. However, with the reduction of minimum feature size, large areas will be needed. Some design strategy has to be adopted in the near future.

### *2.1.2 Operational amplifiers*

Operational amplifiers and operational transconductance amplifiers for switched-capacitors functions can be realized in CMOS process down to a very low supply voltage. Opamps intended to operate at low-voltage conditions with a standard architecture involve three critical points:

- The first is poor dynamic range (DR) due to the reduced supply voltage with no corresponding reduction in device threshold voltage ($V_{th}$).
- The second is low-biasing current due to the reduced gate voltage overdrive ($V_{GS}$-$V_{th}$), where $V_{GS}$ is the gate-source voltage of the input devices.
- The third is limited bandwidth and slew-rate resulting from the low-biasing currents. Therefore, design should focus on maximizing input and output voltage swings and providing high-speed operation.

As the supply voltage is scaled down, the voltage available to represent the signal is reduced; therefore dynamic range becomes an important issue. To maintain the same dynamic range under low supply voltage conditions, the thermal noise in the circuit has to be also proportionally reduced. However, a trade-off has to be made

between noise and power consumption. Because of this important trade-off and under certain conditions, the power consumption will actually increase as the supply voltage decreases. It has been reported that for a given dynamic range (DR) and bandwidth, the power consumption P is inversely proportional to the supply voltage $V_{DD}$ [ABO99a]:

$$P \propto kT \cdot DR\left(\frac{V_{GS} - V_{th}}{\alpha^2 V_{DD}}\right) \tag{2.1}$$

where k and T are respectively the Boltzmann's constant (8.6 x $10^{-5}$ eV/K) and the temperature device junction during the operation in Kelvin (°C + 273.16 °C).

Furthermore, the power is inversely proportional to the square of the fractional signal swing $\alpha$ ($\alpha \leq 1$). Although the supply voltage is a fixed constraint of the technology that cannot be modified, the circuit designer can choose $\alpha$. Thus, to minimize power consumption, it is important to maximize the available signal swing $\alpha$. Several input rail-to-rail ($\alpha$=1) circuit techniques have been proposed [HOG94], [MOT96], [MIN99], [WHI97]. All of them are based on complementary differential pairs (Figure 2.1a) with appropriate control of the tail currents, to keep the transconductance constant. Use of complementary input pairs ensures that at least one pair works properly even when the common mode input signal is close to the rail voltages. Currents generated by the two input differential pairs must be derived to a high impedance node to obtain voltage amplification. The resulting signal is used to drive the output stage. Rail-to-rail output stage, known as class AB, has also been considered as well [WHI97]. Class AB solutions are used in many implementations. They usually

include additional circuits to keep the quiescent current within a given low level. However, at extremely low-voltage supply (1-V and below), a forbidden operation zone arises for input CM voltages in the middle range as shown in Figures 2.1b and 2.1c: the input voltage is not able to turn on any transistor in this range, and therefore the amplifier operation is limited to CM input voltages close to either supply rail.

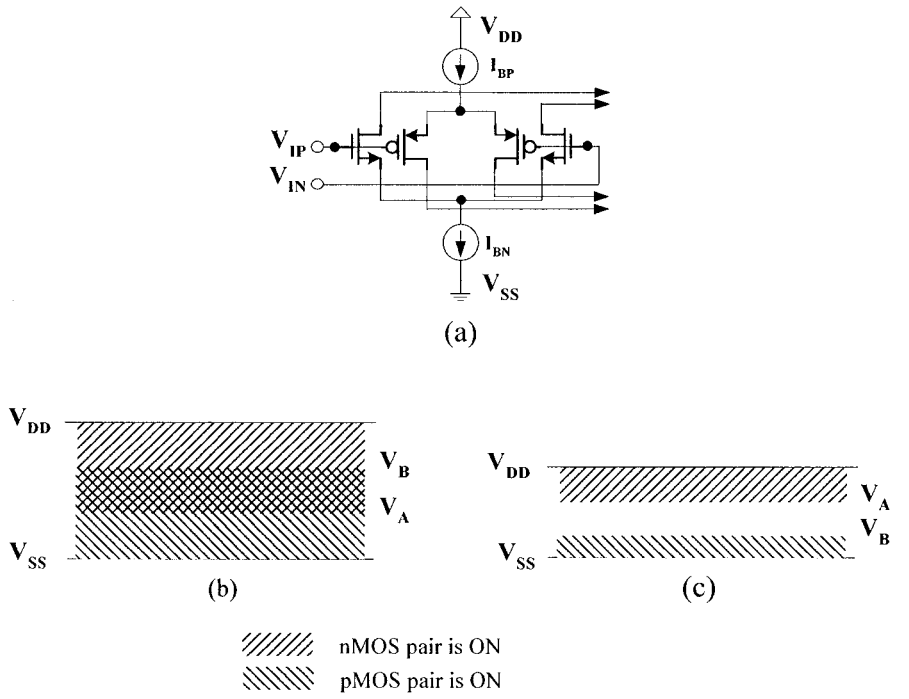


**Figure 2.1:** Rail-to-rail opamp circuit: (a) typical input stage; (b) operation zones for low supply voltage, (c) operation zones for extremely low supply voltage.

These effects are briefly explained below. In a well-designed low-voltage opamp the minimum supply voltage value is imposed by the differential pair of the input stage, and is given by [SAN98]:

$$(V_{DD})_{\min} = |V_{th}| + 2 \cdot |V_{DS,sat}| \tag{2.2}$$

where $V_{th}$ is the threshold of the input stage device and $V_{DS,\,sat}$ is the saturation voltage of the device. For typical CMOS processes, this value turns out to be around 1 V. On the other hand, the main limitation of differential pairs results from the reduced input common-mode (CM) range. For an n-channel input pair, this is given by:

$$V_A < V_{CM} < V_{DD} \tag{2.3}$$

where the lower conduction limits, $V_A$, is defined as

$$V_A = V_{SS} + \left(V_{th,n} + 2 \cdot |V_{DS,sat}|\right) \tag{2.4}$$

$V_{SS}$ and $V_{DD}$ being the negative and positive supply, respectively. The CM of a p-channel input pair is given by:

$$V_{SS} < V_{CM} < V_B \tag{2.5}$$

where the upper conduction band limit, $V_B$, is defined as

$$V_B = V_{DD} - \left(|V_{th,p}| + 2 \cdot |V_{DS,sat}|\right) \tag{2.6}$$

In a well design CMOS opamp, $V_{DS,sat}$ is chosen around 0.2 V in order to keep, the input driven devices, working in strong inversion region. In a 0.18 μm CMOS process the threshold voltage is around 0.5 V. The values of $V_A$ and $V_B$, obtained using Equations

(2.4) and (2.6) are 0.9 and 0.1 V respectively for opamp operating under 1 V supply voltage. Now, a forbidden amplifier operation zone arises for input common mode voltages in the middle range, when using the conventional complementary nMOS/pMOS input differential pair (the input voltage is not able to turn on any transistor pair in this range), leading to the failure of such topology. Therefore, classical solutions have to be replaced by new configurations.

### *2.1.3 Bandgap reference voltage*

One other key component for analog systems is the bandgap reference voltage generator. When properly designed, bandgap reference circuits give an output voltage that is somewhat higher than the material bandgap extrapolated to 0° K; for mainstream CMOS processes $V_{ref} \approx 1.2$ V.

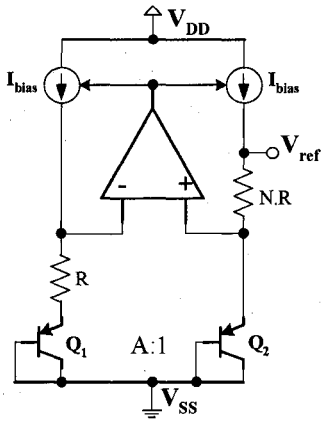


**Figure 2.2:** Typical CMOS bandgap reference circuit.

Typical bandgap reference circuits need at least an extra voltage headroom of 100-300 mV for proper operation, e.g., for the implementation of the current sources in the circuit of Figure 2.2.

The minimum supply voltage for the typical bandgap circuit is then approximately:

$$V_{DD,\text{bandgap ref}} > V_{\text{ref}} + 300\,\text{mV} \approx 1.5\,\text{V} \tag{2.7}$$

With newer CMOS processes, the nominal supply voltage decreases [SIA02] and will continue to decrease with each newer process generation. Clearly, conventional bandgap reference circuits are feasible in CMOS processes until 0.15 μm CMOS generation, provided that the circuit runs at the nominal process supply voltage. For newer CMOS processes, the traditional bandgap reference circuit cannot be used since the supply voltage is too low. The actual situation is even worse for bandgap reference circuits in systems that are operated on supply voltage below the nominal process value to decrease the power consumption of the digital core. Circuit solutions addressing the design issues of bandgap reference voltage at extremely low-voltage (below the nominal process value) will be surveyed in Chapter 3.

### *2.1.4 MOS switches*

Another critical problem in designing switched-capacitor circuits on a low-voltage supply is the difficulty of implementing MOS switches, essential elements for any kind of data converters, used either to sample the analog signal or to perform conversion. In a

typical switched-capacitor circuit, the analog input is sampled through a MOS switch or a transmission gate. The applied voltage to the gate of an nMOS transistor to achieve the ON-state must be higher (or lower for a pMOS device) than the channel voltage by more than the threshold voltage $V_{th}$. If the supply voltage is not large enough and the source (or the drain) voltage of a switch is around the middle of the supply rails, this condition cannot be satisfied and the switch stays off. Ideally, the switch in the on-state acts as a fixed linear conductance $g_{ds}$. In practice, the conductance is strongly signal-dependent as shown in Equation (2.8):

$$g_{ds} = \begin{cases} \left(\mu C_{ox}\frac{W}{L}\right)_n \cdot \left[V_{DD} - V_{th,n} - V_{in} - \gamma_n\left(\sqrt{2\phi_f + V_{in}} - \sqrt{2\phi_f}\right)\right] & \text{nMOS} \\ \left(\mu C_{ox}\frac{W}{L}\right)_p \cdot \left[V_{in} - \left|V_{th,n}\right| - \gamma_n\left(\sqrt{2\phi_f + V_{DD} - V_{in}} - \sqrt{2\phi_f}\right)\right] & \text{pMOS} \end{cases} \tag{2.8}$$

The bulks of the nMOS and pMOS transistors are respectively connected to $V_{SS}$ and $V_{DD}$. Plots in Figure 2.3 are the switch conductance versus input signal $V_{in}$. Figure 2.3a assumes that the supply $V_{DD}$ is much larger than the sum of the two threshold voltages $V_{th,\,n}$ and $V_{th,\,p}$. In this case, it is easy to achieve a large conductance from rail-to-rail for $V_{in}$. When $V_{DD}$ is comparable to the sum of the threshold voltages (Figure 2.3b), there is a substantial drop in the conductance when $V_{in}$ approaches $V_{DD}/2$. Obviously when the power supply $V_{DD}$ is smaller than a critical value $V_{DD,\,crit}$,

$$V_{DD,\,\text{crit}} = V_{th,\,\text{n}} + \left|V_{th,\,\text{p}}\right| \tag{2.9}$$

a gap appears at mid-range, where neither switch conducts (Figure 2.3c).

For reliable design, the maximum electrical field through the oxide must be kept less than a critical value to avoid breakdown mechanism. Reliability aspects have to be taken into account when designing CMOS circuits in deep sub-micron technology. Figure 2.4 shows the forecast gate-oxide thickness as a function of time according to [SIA02]. It displays also the maximum electrical field through the oxide.

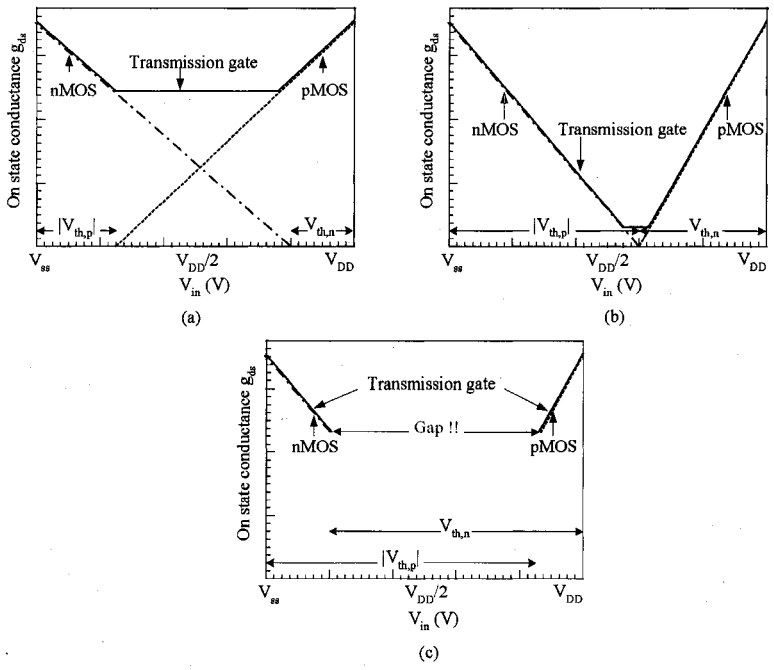


**Figure 2.3:** MOSFET switch conductance versus the input signal using various supply voltage: (a) regular, (b) near critical supply, (c) below critical supply.

An approximated estimation of the gate-oxide thickness as a function of feature size is given by [MEA94]:

$$t_{ox} = 210 \cdot L^{0.77} \tag{2.10}$$

where the feature size is in μm and the gate oxide thickness is in Å.

Methods to overcome the MOS switches implementation problem can be divided into two categories: technology-based and circuit-based. The technology-based method use low threshold transistors, whereas the circuit-based methods increase the overdrive voltage while taking into account the circuit reliability issues. The circuit-based approach has been adopted in this thesis. New design strategies were developed as there are limits in reducing oxide thickness.

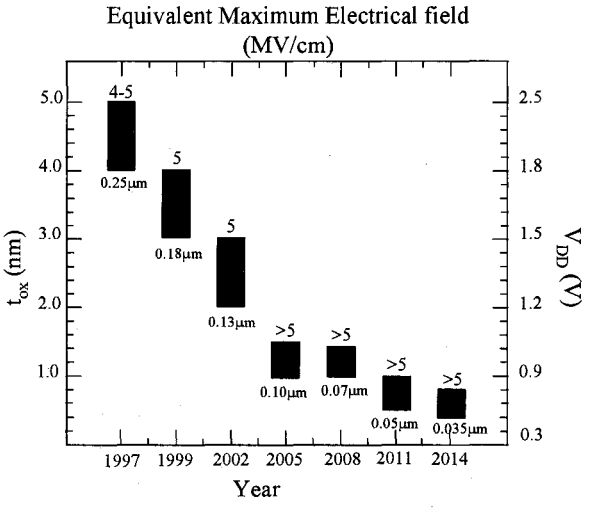


**Figure 2.4:** MOS gate-oxide thickness and maximum electrical field as a function of time [SIA02].

## 2.2 Low-voltage CMOS analog circuits and reliability

Reduced power supply voltage level does not necessarily lead to lower power dissipation for analog circuits, but it should be recommended. Over the years, users have asked for more reliable electronic equipment. At the same time, electronic equipment

has evolved and become ever more complex. The combination of these two factors has put great emphasis on the need to ensure bug-free operation over a long period. To design within the reliability limits of the technology, the technological parameters and limits must be well known.

Circuit aging refers to the deterioration of circuit performance over time. This time duration can be a few years or even a few months under worst-case conditions. Circuits have always aged but, this aging worsens until the latest iteration of Moore's law, which pushed transistor channel lengths below 0.09 μm. The simultaneous use of extremely small channel lengths and higher operating frequencies has elevated circuit aging from an academic exercise to a growing, and perhaps detrimental, concern for system-on-a-chip (SoC) designs. Circuit aging can no longer be ignored. All portions of the SoC, whether analog, digital, or memory, will be affected. These negative impacts can include slower speeds, irregular-timing characteristics, and increased power consumption. In extreme cases, circuit aging may even cause functional failures to occur over time.

The predominant cause of circuit aging is the degradation of individual deep submicron transistors. This phenomenon, known as hot-carrier-induced (HCI) degradation, has been extensively studied since the early 1980s. A transistor conducts when carriers are sent from one side of the transistor, known as the source, to the other side, the drain. The force that propels these carriers is called the electric field. In very deep submicron transistors, these electric fields become much more intense. As a result, the carriers travel much faster, leading to the increase in speed. Such speeds, however,

come with a price. The carriers have been accelerated so much and travel so fast that upon their arrival at the drain side of a transistor, they literally shatter the surrounding silicon atoms. The violent collisions that occur, called impact ionization, result in the splitting of each atom into two new carriers: one electron and one hole (Figure 2.5). The longer the transistor is in operation, the greater the number of new carriers that are generated. Both HCI and circuit aging are cumulative behaviors over time. The newly created carriers could be tolerated if they did not damage the physical structure of the transistor. Unfortunately, they do harm. In the nMOS-type transistors, the electrons inflict damage to a particular area, between the gate oxide and the silicon surface. This interface can become populated with so-called interface "states" causing the nMOS transistor to have higher threshold voltages. As a result, the device produces less current which translates into slower switching speeds. The exact amount of this decrease can be quantified by measuring the newly created holes that flow out through the silicon substrate (represented by $I_{SUB}$). For pMOS transistors, the degradation mechanism is a little different. The newly created electrons are at fault once again. This time, though, they lodge and trap themselves inside the gate oxide of the transistor. Such electron trapping causes the pMOS transistor to have lower threshold voltages. As a result, pMOS transistors will have more current than before HCI degradation. The monitor for pMOS transistors is its gate current (represented by $I_{GATE}$). The precise level of degradation for a transistor is a complex function of its bias or operating conditions.

Usually, a fixed level of device degradation is assigned. The time to reach this is used to gauge the robustness of the technology to HCI degradation

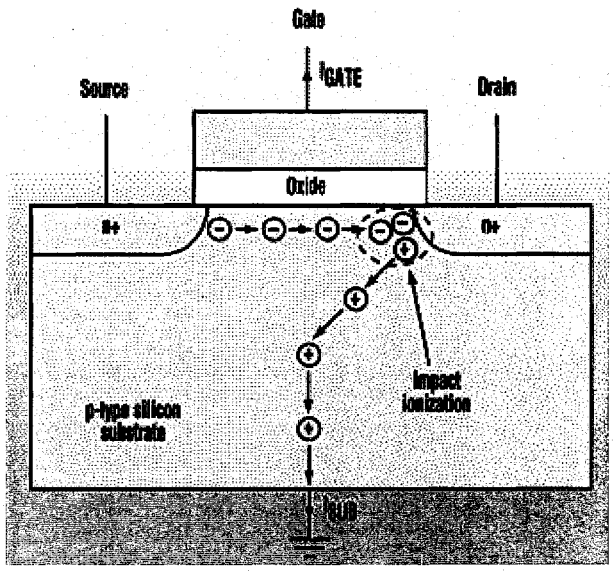


**Figure 2.5:** Hot carrier induced phenomenon [CHE00].

For example, it might take five months to reach a 10% change in the drain current of a transistor. Therefore, the lifetime of the transistor would be five months. For the past 15 years, lifetimes have rapidly decreased from roughly 10 years to just a few months (Figure 2.6). This downward spiraling trend has caught the attention of many semiconductor manufacturers, and is indicative of the severity of HCI and circuit aging. Circuit aging is an unavoidable consequence of very deep submicron (VDSM) technology. The breadth and depth of its degradation will only expand as designs use smaller transistors and operate at faster speeds. Critics have argued that lowering the level of the power supply with each successive semiconductor-technology generation

will significantly lower the electric fields inside each transistor. Furthermore, they claim this will make HCI and circuit aging disappear.

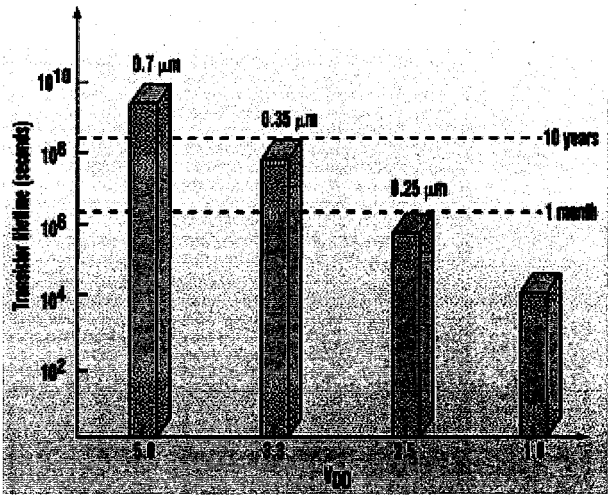


**Figure 2.6:** Transistor lifetime as a function of supply voltage [CHE00].

But, evidence proves otherwise. Incremental drops in power-supply voltage simply aren't enough to offset the rigorous pace of Moore's law. Electrical fields inside transistors tend to increase thus HCI effects worsen and designers must be aware of that. Equations for quantifying those phenomena will be given below.

### *2.2.1 Physical limits on devices*

The signal processing capabilities of a device can be measured by its frequency response (speed of operation) and dynamic range (bit accuracy). It has been shown [NAG92] that the ultimate performance limits of a transistor are set by this equation:

$$V_m \cdot f_t = \frac{E_{bd}}{2\pi} \cdot v_s \tag{2.11}$$

where $V_m$ is the maximum oxide voltage allowable applied to the device, $f_t$ is the cutoff frequency of the device, $E_{bd}$ is the electrical field in the oxide that causes breakdown and $v_s$ is the saturated drift velocity of the carrier in the device material. Since $f_t$ and $V_m$ represent the operating speed and proportional to the dynamic range of the device, respectively, the product represents the total signal processing capability of the device, which is limited by the characteristics of the material as seen on the right. Thus, a semiconductor device has the maximum physical capability allowed by its material, and the operating speed and voltage, or the dynamic range, must be a trade-off.

Oxide breakdown, gate induced drain leakage, hot electron effects, and punch-through can all induce CMOS circuit failure [ABO99a]. Important results obtained in [ABO99a] will be reported here for convenience. CMOS technology is typically designed such that all these failure modes occur at a same stress level, which is an important factor determining the rated supply voltage. Then, if the following device voltages are kept within the rated supply voltage, a long circuit lifetime can be assured with high confidence. Instantaneous and time-dependent gate-oxide breakdowns limit the gate-source and gate-drain potential differences that can be applied to a transistor. Based on constant voltage tests on small-area oxides (area < $400\mu m^2$), the time-to-breakdown $t_{bd}$ has been shown to follow the reciprocal field dependence [MOA90]:

$$t_{bd}(T) = \tau_0(T) \cdot \exp\left( G(T) \cdot \frac{t_{ox}}{V_{ox}} \right) \tag{2.12}$$

where $t_{ox}$ is the gate-oxide thickness, $V_{ox}$ is the voltage across the oxide, G(T) and $\tau_0(T)$ are temperature dependent parameters which are respectively $10^{-11}$ s and 350 MV/cm for T=300 K. The voltage across the oxide must be chosen such that:

$$V_{ox} < E_{bd} \cdot t_{ox} \tag{2.13}$$

where $E_{bd}$ is the breakdown electrical field across the oxide.

For a lifetime of 30 years, $E_{bd}$ is typically 5 MV/cm [MOA90]. It has also been reported [MOA90] that the gate-induced drain leakage tunneling current limits the voltage across the oxide. To keep that leakage to a reasonable value, the gate-drain voltage must be limited as follows:

$$V_{GD} < E_{GIDL} \cdot t_{ox} + 1.2V - V_{FB} \tag{2.14}$$

where $E_{GIDL}$ is electric field in the oxide that induces tunneling (typically 4 MV/cm), 1.2 V is the bandgap voltage and $V_{FB}$ is the MOSFET flat-band voltage (approximately 0 V for n+ poly over n+ drain; and 1.1 V for n+ ploy over p+ drain). GIDL occurs when the gate is grounded (device cutoff) and the drain is a high-voltage. Thus for a nMOS device, a depletion region is formed in the n+ drain. If the drain voltage is high enough, an inversion layer of holes will begin to form.

When the device is on, hot-electron effects can damage the device and degrade performance over time, limiting the $V_{DS}$ and $V_{GS}$ that can be applied. This constraint is described by [ABO99b]:

$$V_{DS} < V_{DS,sat}(L) + E_C \cdot (L_2 + L_{LDD}) \tag{2.15a}$$

with $L_2$ given by [ABO99b]:

$$L_2 = 0.2 \cdot t_{ox}^{1/3} \cdot X_j^{1/2} \tag{2.15b}$$

where $V_{DS.\,sat}$ is the saturation voltage of the device (which is a function of the bias and channel length L), $E_C$ is the critical electric field, $L_{LDD}$ is the effective length of the lightly doped drain and $X_j$ is the drain-source junction depth.

Finally, punch-through voltage $V_P$, limits the magnitude of $V_{DS}$ when the device is off and is described by [ABO99b]:

$$V_{DS} < V_P \propto \frac{N_{sub} \cdot L^3}{X_j + 3 \cdot t_{ox}} \tag{2.16}$$

where, $N_{sub}$ is the substrate doping concentration.

Critical terminal voltages $V_{GS}$, $V_{GD}$ and $V_{DS}$ must be kept within the rated operating voltage supply $V_{DD}$ of the technology to ensure device reliability. Terminal voltages are only relative to each other and not to an absolute reference such as ground. This has to be taken into account during the implementation of the state-of-the-art circuitry.

### *2.2.2 Power and temperature limits on circuits*

An important limitation is the maximum temperature at which a semiconductor functions properly. Assuming that electrical conditions remain within specifications, Arrhenius equation [LAK99] below models the rate of electrical failures R, induced by temperature:

$$R = A \cdot \exp\left(-\frac{E_a}{kT}\right) \tag{2.17}$$

where A, $E_a$ (eV), k and T are respectively an empirical constant, activation energy (eV), Boltzmann's constant (8.6 x $10^{-5}$ eV/K) and the temperature device junction during the operation in Kelvin (°C + 273.16 °C).

As temperature increases (due to large power dissipation), so does the failure rate, thus, more devices fail at higher temperatures than at lower ones. Arrhenius equation provides a tool for estimating the failure rates. Different failure mechanisms have different activation energies that range from 0.3 eV to 1.3 eV as shown in table 2.1, but temperature remains the factor that can accelerate failure mechanism.

Contribution of oxide defects in failure mechanism, is important than that of charge injection at high temperature as depicted in Table 2.1 . The designer has control on mechanisms such as charge injection which can be minimized during circuit implementation. The effects of other stresses can be determined using other models. The Eyring equation models thermal and environmental mechanisms. Lawson model, and the Peck equations model the effects of temperature and humidity [AJI99], [CHE00].

**Table 2.1:** Failures mechanism activation energies [LAK99].

**Activation Energies for Failure Mechanisms**

| Failure Mechanism | Activation Energy, $E_a$ (eV) |
|---|---|
| Oxide defects | 0.3 to 0.5 |
| Bulk silicon defects | 0.3 to 0.5 |
| Corrosion | 0.45 |
| Assembly defects | 0.5 to 0.7 |
| Electromigration | 0.6 (Al line), 0.9 (Contact) |
| Mask or photoresist defect | 0.7 |
| Contamination | 1.0 |
| Charge injection | 1.3 |

By applying these models, the rate at which a specific mechanism will cause devices to fail can be determined in advance. If devices seem to fail at a particularly high rate, the models can help to gain insight into the conditions that users have subjected them to.

The power dissipated in a circuit increases its temperature because there is a thermal resistance between a device and its environment. The integration level $N_G$ (gates/chip) and the speed $t_{pd}$ (switching time) of an integrated circuit must observe the following relationship [NAG92]:

$$\frac{N_G}{t_{pd}} \leq \frac{\Delta T}{\theta E} \tag{2.18}$$

Here $\Delta T$ is the maximum temperature rise between a device and its environment, $\theta$ is the thermal resistance between them, and E is the switching energy of each gate. Relation (2.18) shows that VLSI performance and cost- that is, speed and packaging density- are limited by the quantity on the right side, which are closely related to the packaging system and the rates of heat production and dissipation. The laters play an important role in the reliability of the system.

For a high-performance VLSI, $\Delta T/\theta E$ should be as large as possible. There is a little difference in $\Delta T$ and $\theta$ between bipolar and CMOS VLSI's because both are made of the same materials. Values of E, however, depend upon device structures and circuit configurations. It should be noted that $\Delta T$, $\theta$ and E are of equal importance in VLSI performance, that there is a trade-off between the speed and integration level in a

cooling limited situation, and that the value is limited by the switching energy of the circuits and the packaging conditions.

If typical values of $\Delta T = 100$ °C, $\theta = 2.5$ °C/W and $E = 0.1$ pJ are used, then

$$\frac{N_G}{t_{pd}} \leq 4 \times 10^5 \text{ (gates/ns)} \tag{2.19}$$

In other words, the maximum number of gates on a chip, if all the gates are operating, must be less than 0.4 M if the switching speed of each gate is 1 ns, when the switching energy is 0.1 pJ and the power dissipation of the chip is 40 W!! (too high). In a real system all the gates are not operating simultaneously. The maximum number of gates on a chip could be considerably larger than this, but still there is a limitation.

The effects of CMOS technology and supply voltage on the most commonly used analog blocks has been analyzed and reliability issues addressed in this chapter. In a well-designed circuit, these effects have to be considered and become a design constraint. In the next chapter, low-voltage analog circuits in deep submicron CMOS will be reviewed.

# *Chapter 3*

# *LOW-VOLTAGE ANALOG CIRCUITS IN DEEP SUBMICRON CMOS: A REVIEW*

Improvements in CMOS technology, operating at ever-increasing frequencies and lower supply voltages, and the scaling down of the minimum size of transistors tend to reduce the available voltage swing of analog circuits. One way of overcoming this problem is to use low threshold technologies, another is to find improved and simple circuits techniques permitting the dynamic range of analog circuits to be increased. The latter will be the subject of this chapter. Reliability constraints of scaled CMOS technology is briefly discussed in Chapter 2. We do not intent to present a review of state-of-the-art technology, but we do describe briefly almost all low-voltage design techniques suitable for analog circuits structure in standard CMOS process along with their merits and demerits. An extended survey on reliable circuit techniques for low-voltage analog design in deep submicron standard CMOS has been covered in a journal paper submitted to Analog Integrated Circuits and Signal Processing [FAY03a] and is in press. This discussion focuses specially on CMOS design for achieving high dynamic range circuit. Bandgap reference voltage circuits will be also covered.

## 3.1 CMOS bandgap reference circuits

By definition a bandgap reference (BGR) is a voltage reference of which the output voltage is referred to the bandgap energy of the used semiconductor. The first bandgap reference was proposed by Robert Widlar in 1971 [WID71] and used conventional junction isolated bipolar technology to produce a stable low-voltage (1.25 V). Reference voltage generators are used in DRAM's, flash memories and analog devices and must be stabilized over process, voltage and temperature variations, and also must be implemented without modification of fabrication processes [KUI73]. As the demand for low-power and low-voltage operation is strongly increasing the spread of battery-operated portable applications, this fixed output voltage of 1.25 V limits the low $V_{DD}$ operation (1-V and below).

In order to operate a BGR at supply voltages lower than the material bandgap, a straightforward solution is to make bandgap reference circuits with an output lower than the silicon of the material bandgap. If first-order temperature insensitivity is to be guaranteed, this implies that diodes with low material bandgap must be used. Following are the three ways to achieve this:

i. Introducing a low-bandgap material (e.g., germanium) to make the low-bandgap diodes in the BGR circuit. This option is very expensive and is not available in standard CMOS processes.

ii. Using the total voltage across the diodes by composing the electrical field across the junction from the externally applied voltage and an electrostatic

field. The bandgap "seen" by the circuit equals the material bandgap lowered by the electrostatic field. In standard digital CMOS process, this method is not usually used, despite the fact that it requires less area and little power because no resistors have to be used. The way to implement this method is to replace the normal diodes by MOS diodes with an interconnected gate and backgate. This device is called dynamic threshold MOS transistor or DTMOST [ASS94], [SRI00] and is used by Annema [ANN99b].

iii. Using a fraction of the voltages across the diodes instead of the total voltages by resistive subdivision [BAN99], [BOE01], [JIA00], [LEU02], [MAL01], [MIE97], [NEU97]. By doing so, the bandgap as "seen" by the circuit is also a fraction of the material bandgap. To achieve a virtual low bandgap using resistive subdivision, a number of high value ohmic resistors are needed for low-power applications. This results in considerable area consumption.

Most state-of-the-art implementations make use of the latest method as summarized in Table 4.1. From this table, technologies with low $V_{th,n}$ are required in [JIA00] and [NEU97] while native nMOS transistors are needed in [BAN99]. DTMOST is used in [ANN99b], and BiCMOS process is used in [MAL01]. The main reason for these approaches is to overcome the problem of input common-mode voltage of the error amplifier in the proportional-to-absolute-temperature (PTAT) current generation loop. The method described in [LEU02] solves this problem with sub-1-V supply operation and provides comparable performance. It is therefore clear that opamp design is the limiting factor on the minimum supply requirement for most of those circuits.

**Table 3.1:** Low-Voltage Bandgap References

| | Technology | Threshold Voltage (V) | Min $V_{DD}$ (V) | Supply Current (μA) | $V_{ref}$ (mV) | TC (ppm/°C) |
|---|---|---|---|---|---|---|
| [LEU02] | 0.6-μm CMOS | $V_{th,p}$=-0.9<br>$V_{th,n}$= 0.9 | 0.98 | 18 | 603 | 15 |
| [MAL01] | 0.8-μm BiCMOS | - | 0.95 | < 92.0 | 536 | 19 |
| [JIA00] | 1.2-μm CMOS | $V_{th,p}$=-0.91<br>$V_{th,n}$= 0.53 | 1.2 | ~ 500 | ~ 1000 | ± 100 |
| [BAN99] | 0.4-μm CMOS | $V_{th,p}$=-1.00<br>$V_{th,n}$= 0.70<br>$V_{th,I}^{+}$ = -0.20 | 2.10<br>(♣ 0.84) | 2.2 | 515 | ± 59 |
| [MIE97] | | - | - | - | 600 | - |
| [NEU97] | 0.8-μm CMOS | $V_{th,p}$=-0.70<br>$V_{th,n}$= 0.50 | 0.90 | - | 670 | - |
| [ANN99] | 0.35-μm CMOS | $V_{th,p}$=-0.65<br>$V_{th,n}$= 0.65 | 0.85 | < 1.2 | 650 | 57 |

## 3.2 Other low-voltage techniques and analog building blocks

Basic analog building blocks (opamp and analog switches) implementation for low-voltage design is covered in this section with the implementation of MOS capacitors. The pertinent literature on low-voltage operational amplifier is surveyed (including some of the main contribution of this thesis) and techniques for operation at low power supply voltages are identified. Please note this section is in press for the *Kluwer Academic Publishers* journal Analog Integrated Circuits and Signal Processing.

### 3.3 Reliable Circuit Techniques for Low-Voltage Analog Design in Deep Submicron Standard CMOS: A Tutorial

# Reliable Circuit Techniques for Low-Voltage Analog Design in Deep Submicron Standard CMOS: A Tutorial

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Journal: *Kluwer Academic Publishers* Analog Integrated Circuits and Signal Processing

Status: Submitted on August 2001, Revised on February 2003, Accepted on May 2003

**Abstract**

We present in this paper an overview of circuit techniques dedicated to design reliable low-voltage (1-V and below) analog functions in deep submicron standard CMOS processes. The challenges of designing such low-voltage and reliable analog building blocks are addressed both at circuit and physical layout levels. State-of-the-art circuit topologies and techniques (input level shifting, bulk and current driven, DTMOS), used to build main analog modules (operational amplifier, analog CMOS switches) are covered with the implementation of MOS capacitors.

**Key Words:** Reliable Low-Voltage CMOS Analog Design, deep submicron, bulk driven and current driven bulk opamp, DTMOS, CMOS switches.

# I. INTRODUCTION

The general trend in CMOS technology is to make the devices smaller and smaller to increase the density and speed of digital circuits. It is also common to reduce the thickness of the gate oxide in order to increase the driving capability of the transistor. In addition, the thickness reduction implies that the supply voltage must be decreased to avoid excessive electric field in the devices. Three main reasons can be given for the advent of low-voltage circuits. As the channel length is scaled down into submicrons and the gate-oxide thickness becomes only several nanometers thick, the supply voltage has to be reduced (down to 1.5 V and below in the near future) [1] in order to ensure device reliability. The second reason emanates from the increasing number of components on a single chip. A silicon chip can only dissipate a limited amount of power per unit area. Since the increasing density of components allows more electronic function per unit area, the power per electronic function has to be lowered in order to prevent overheating of the chip. The third reason is dictated by portable, battery-powered equipment. In order to have an acceptable operation period from a battery, both the supply power and the supply voltage have to be reduced. Reduced power supply voltage is normally not an advantage for analog design and a low supply voltage may require some special circuit techniques. Such techniques will be covered in this paper. Emphasis will be on circuit level aspects. Trends in technology as well as the process impact are extensively discussed by Klass Bult in [1] and will not be covered here. State-of-the-art techniques suitable for almost rail-to-rail low-voltage operational amplifier (input level shifting, bulk driven and current driven bulk, DTMOS) as well as

analog CMOS switches are the main focus of Section II. The implementation of MOS capacitors using fringing effects, floating and depletion mode device will be covered in Section III and we conclude with Section IV.

## II. Low-Voltage Deep Submicron Analog Building Blocks

Basic analog building blocks (opamp and analog switches) implementation for low-voltage design is covered in this section.

### A. Low-Voltage operational amplifier

One of the most important basic building block in analog and mixed-mode circuits is the operational amplifier. In a low-voltage (LV) opamp, the minimum supply value is imposed by the differential pair of the input stage and is equal to the threshold voltage ($V_{th}$) plus two overdrive voltages ($V_{DSat}$). In typical CMOS processes, this value turns out to be around 1-V. On the other hand, the main limitation of differential pairs is the reduced input common-mode range (ICMR). In order to minimize the supply requirements of the input stage, both input terminals of an opamp must work with potentials very close to one of the supply rails. To overcome this limitation, several schemes for discrete-time (switched) operation with a single supply down to 1 V and large output signal swings have been recently reported [2]-[10]. The switched-opamp (SO) technique [2] has been shown to be a promising low-cost solution to realize switched-capacitor (SC) circuits in standard CMOS processes. The SO eliminates critical MOS switches that set the minimum supply voltage to allow sub-1-V operation of the SC circuits [4] and, thus, does not have a reliability problem. Since then, a few

modifications have been proposed to improve the performance of the SO techniques in terms of operation speed and compatibility with existing SC circuits. In switched applications, no input swing is required for the opamp since both input terminals operate at one of the supply rails. Many others 1 V opamps are continuous-time for differential operation but use switches for the common-mode. These techniques will not be covered in this paper. Most of continuous-time techniques will be addressed and can be classified in three categories.

**Table 3.2:** Trends in Low-Voltage CMOS opamp.

| **Method** | Authors | Technology | Threshold Voltage (V) | Gain (dB) | UGB (MHz) $C_l$ = load capacitor | Power (μW) | $V_{DD}$ (V) |
|---|---|---|---|---|---|---|---|
| Common-mode Level Shifting | Fayomi et. al [11] | 0.18-μm CMOS | $V_{th,p}$=-0.48 $V_{th,n}$= 0.52 | 60 | 26.6 ($C_l$ = 5pF – $R_l$ = 20kΩ) | 400 | 1 |
| | Karthikeyan et. al [13] | 1.2-μm CMOS | $V_{th,p}$=-0.8 $V_{th,n}$= 0.60 | 60 | 10 ($C_l$ = 20 pF – $R_l$ = 10kΩ) | 150 | 1 |
| | Lee et. al [14] | 1.2-μm CMOS | $V_{th,p}$=-0.8 $V_{th,n}$= 0.60 | 58 | 2.2 ($C_l$ =20 pF) | 400 | 1 |
| | R-Angulo et. al [15] | 0.8-μm CMOS | $V_{th,p}$ ≈-0.85 $V_{th,n}$ ≈ 0.85 | - | 13 ($C_l$ = 10 pF) | 70 | 1.2 |
| | R-Angulo et. al [16] | 0.8-μm CMOS | $V_{th,p}$ ≈-0.85 $V_{th,n}$≈ 0.85 | 60 | 5 ($C_l$ = 50 pF) | - | 1.2 |
| | D-Carillo et. al [17] | 1.2-μm CMOS | $V_{th,p}$ ≈-0.75 $V_{th,n}$≈ 0.75 | 87 | 1.9 ($C_l$ = 15 pF) | 410 | 1 |
| Bulk-driven | Blalock et. al [19] | 2.0-μm CMOS | $V_{th,p}$ ≈-0.80 $V_{th,n}$≈ 0.80 | 44.8 | 1.3 ($C_l$ = 22 pF) | 287 | 1 |
| Current driven bulk | Lehmann et. al [20] | 0.5-μm CMOS | $V_{th,p}$ ≈-0.60 $V_{th,n}$≈ 0.60 | 62 - 69 | 2 ($C_l$ = 20 pF) | 40 | 1 or less |
| DTMOS | Annema [29] | 0.35-μm CMOS | $V_{th,p}$=-0.65 $V_{th,n}$= 0.65 | - | - | 1.2 | 1 or less |

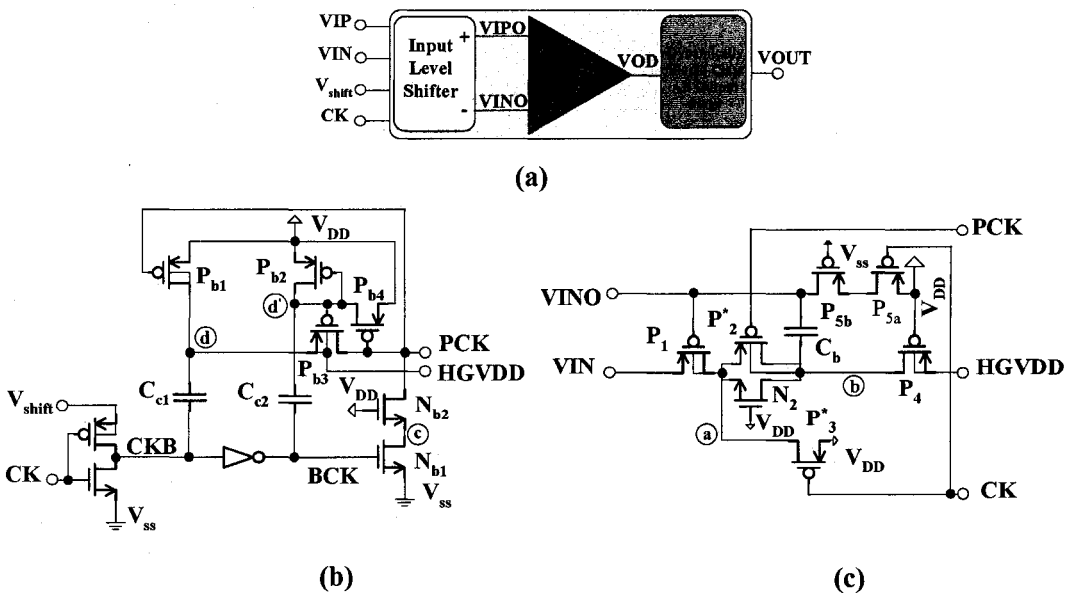
The first technique is mostly based on level shifting of the common input signal to a value capable of driving the input terminals [11]-[18]. Continuous-time and switched-

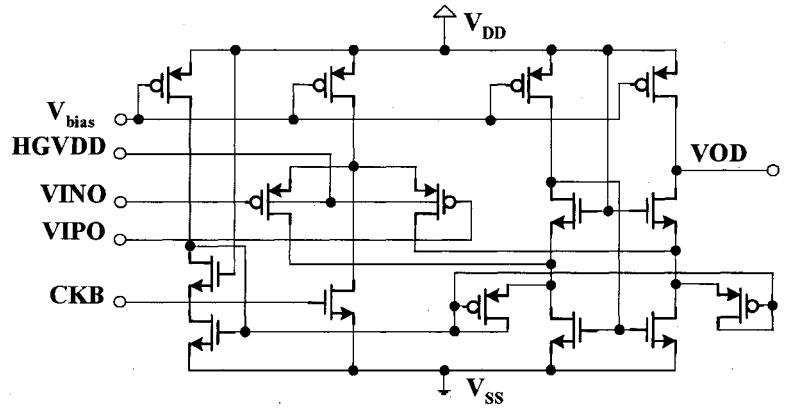
capacitor techniques have been developed to shift the input. The second concept makes use of the bulk-driven MOS transistor [19]-[20] and current driven bulk [21] techniques, while the local charge pump based approach is described in [22]. The latter technique will not be addressed since it is not widely used. Table 3.2 gives a simplified overview of the methods used for achieving almost rail-to-rail low-voltage opamp designs with their related performance. Detailed description will be given below.

## 1. Common mode level shifting opamp based method

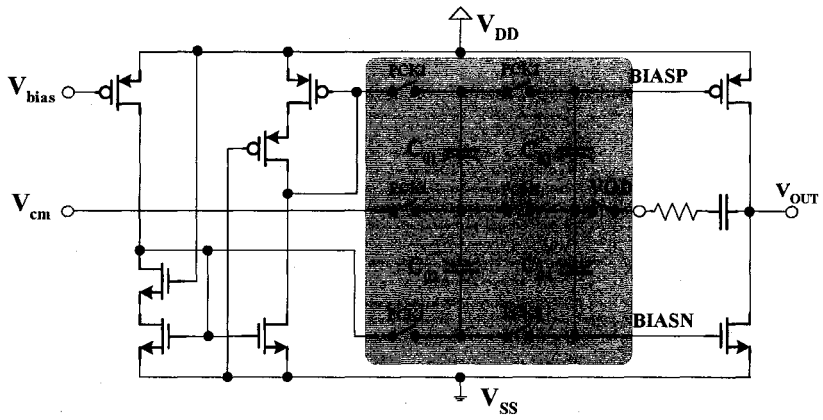
In these approaches, the opamp input common-mode voltage is set to a voltage closed to $V_{SS}$ or $V_{DD}$.

In [11] a switched-capacitor technique is used to level-shift down the common-mode input voltage (Figure 3.1(a), 3.1(b) and 3.1(c)).






(b)




(e)

**Figure 3.1:** Low-voltage CMOS opamp using switched-capacitor level-shifter: (a) block diagram, (b) Clock booster, (c) pMOS level shifter, (d) pMOS input stage, (e) dynamically biased class-AB output stage.

The level-shifter circuit is followed by a pMOS driven input differential pair (Figure 3.1(d)) with a dynamically biased class AB output stage (Figure 3.1(e)) to ensure a rail-to-rail input/output functionality of the opamp. The level shifter circuit

makes use of the control circuit of a pMOS bootstrapped constant impedance switch (Figure 3.1(b)) described in [12]. When the clock signal is low, the gate voltage of the pMOS type input differential transistor is set to $V_{DD}$ and therefore is off. At the same time node b is set to $V_{DD} + V_{shift}$. The charge $Q_{CH1}$ stored in capacitance $C_b$ is given by:

$$Q_{CH1} = C_b V_{shift} \tag{3.1}$$

where $V_{shift}$ , is an arbitrary voltage greater than the threshold of the pMOS input pair devices.

When the input clock signal goes high, the transmission gate formed by $N_2$ and $P^*_2$ starts conducting the input signal $V_{IN}$. Charge stored in capacitance $C_b$ thus becomes:

$$Q_{CH2} = C_b(V_{IN} - V_{INO}) \tag{3.2}$$

Using the charge conservation principle, the input drive voltage of the differential pair can be derived from (3.1) and (3.2) and is given by:

$$V_{INO} = V_{IN} - V_{shift} \tag{3.3}$$

Equation (3.3) shows that a linear relation exists between the input signal and the control voltage of the differential pair. The input voltage is therefore level-shifted down. The value of this voltage is low enough to turn on the differential pair at any input CM level and therefore suppresses the forbidden operation zone of the opamp. The input CM is typically between -1 and 0 V for an input signal varying from 0 to 1 V and for a $V_{shift}$ equal to 1 V. Reliability is not a concern since a 1.8 V technology is used at a 1 V supply voltage. The transfer function of the level-shifting block is linear. Figure 3.2

sketches the input-output response of the circuit. $V_{shift}$ is an arbitrary value that is fixed so as to be able to drive the input differential pair. The operation principle of the remaining blocks is clearly described in [8]. The amplifier is capable of operating with a power supply as low as 1-V while providing a 26.6 MHz unity gain frequency and a 67-degree phase margin with a load condition of 5 pF and 20 kΩ. The circuit dissipates 400 μW.

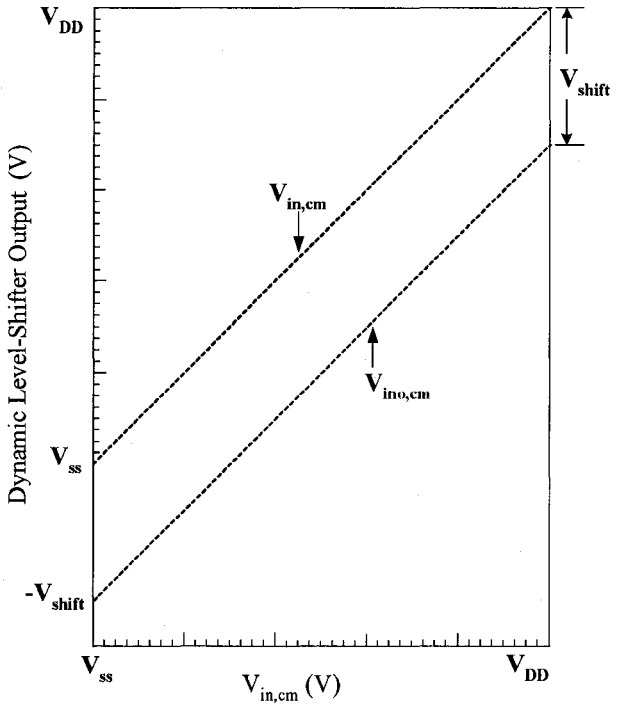



**Figure 3.2:** Level Shifter transfer function.

Analog circuit using inverting opamp configuration can be converted into low-voltage topology by biasing the opamp input common-mode voltage to near one of the

supply rails [13]. In this technique, a current source $I_B$ is introduced as shown in Figure 3.3(a).

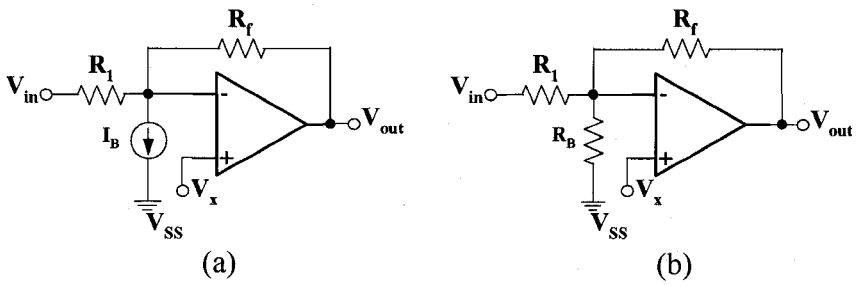



**Figure 3.3:** Biasing schemes for low-voltage CMOS opamp in a single-ended configuration using: (a) a current source and (b) a resistor.

If the input and output quiescent voltages are equal to $V_{DD}/2$, thus the required current $I_B$ is given by:

$$I_B = \left(\frac{V_{DD}}{2} - v_x\right)\left(\frac{1}{R_1} + \frac{1}{R_f}\right) \tag{3.4}$$

Since $I_B$ is most conveniently realized using an nMOS, the value of $v_x$ has to be greater than $V_{DS,sat}$, and hence the minimum supply voltage of the circuit is $V_{DS,sat}+2V_{SD,sat}+|V_{th,p}|$. If the input stage of the opamp is realized using nMOS differential pair, setting $v_x$ close to $V_{DD}$ with a pMOS current source $I_B$ connected between the opamp negative input terminal and $V_{DD}$ will minimize the supply voltage. A resistor or a MOSFET operating in the triode region can be used to bias the opamp input common-mode voltage as shown in Figure 3.3(b). The resistance $R_B$ can be determined as:

$$R_B = \frac{v_x}{\frac{V_{DD}}{2} - v_x}\left(R_1 // R_f\right) \tag{3.5}$$

The second approach has the advantage of setting $v_x$ to a value lower than one $V_{DS,sat}$ (but greater than the ground). The method can be extended to convert a fully differential inverting opamp configuration into a low-voltage design. In this case, two current sources or two resistors are required to connect to the fully differential opamp inputs, and the values of the current sources or resistors can be determined based on the input and output common-mode voltages. Adding the current source or resistor induces minimal effects on the low frequency response since they are connected to the virtual ground of the opamp. However, at high frequency, the bandwidths of the two schemes are different. The obtained reduction in supply voltage, however, comes with a price of increasing the overall noise. The mean squared output noise $v^2_{no}$ for both circuits shown in Figure 3.3 can be written as:

$$v_{no}^2 = \left(I_{n1}^2 + I_{nf}^2 + I_n^2\right)R_f^2 + v_{na}^2\left(1 + \frac{R_f}{R_1 // R_x}\right)^2 \tag{3.6}$$

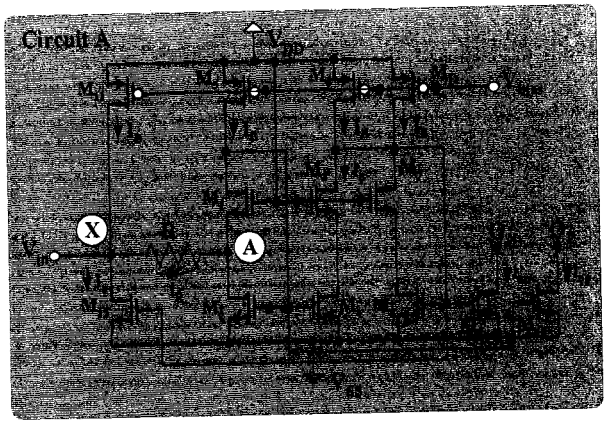
where $I_{n1}$, $I_{nf}$ and $v_{na}$ are the equivalent noise currents of $R_1$, $R_f$ and the equivalent noise voltage of the opamp respectively. When compared to the case without the addition of $R_B$ and $I_B$, additional terms $I^2_n$ and $R_x$ are presented in (3.6). For Figure 3.3(a), $R_x$ is equivalent to $r_{ds}$, and $I^2_n$ is due to the noise current of $I_B$. With $v_x = V_{DS.sat}$, $I^2_n$ can then be derived using (3.4) as

$$I_n^2 = \frac{16}{3} kT \frac{\frac{V_{DD}}{2} - v_x}{v_x \left( R_f // R_1 \right)} \tag{3.7}$$

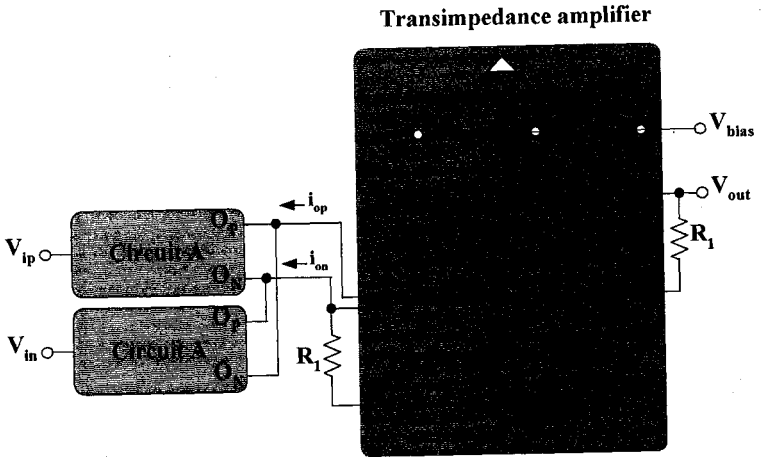
where only thermal noise is considered. For Figure 3.3(b), $R_x$ is equal to $R_B$, and $I^2_n$ is due to the equivalent noise current of $R_B$ that can be also described using (3.7) except that the scaling factor 16/3 is now equal to 4. In most cases, the term due to the opamp noise $v^2_{na}$ is usually the dominant factor. Since $R_B < R_1 < r_{ds}$, the circuit shown in Figure 3.3(a) has lower noise than the circuit shown in Figure 3.3(b). Furthermore, due to the term $I^2_n$, it has a slightly higher noise than the case when either $R_B$ or $I_B$ is omitted. Additional analysis of the noise performance can be found in [13]. Opamp implemented in [13] using this technique settles to 0.1% accuracy in about 120 ns under a 1-V power supply. This technique can be used for interfacing circuits that require higher voltage. This is possible since there is no limit on the voltage range at the input of the resistor, except the limit posed by the input protection diodes in the ESD.

In [14], a low-voltage (1-V and below) transconductor circuit (Figure 3.4(a)) has been introduced and used to build the opamp circuit (Figure 3.4(b)). The current $i_R$ in the transconductor is given by the change in the input signal $v_{in}$ divided by R (since A is a low-impedance node) and is mirrored to the output node $O_P$ as $i_{op}$. Transistors $M_{11}$ and $M_{12}$ are introduced to boost the input impedance at node X. For practical implementation, transistor mismatch and the finite output impedance of $M_6$ and $M_{13}$ (Figure 3.4a) will affect the matching between $i_x$ and $i_R$. As a result, the output impedance of transistors $M_{11}$ and $M_{12}$ usually determines the input impedance of the

transconductance and is limited to about 100-200 kΩ. Another effect that will be caused by transistor mismatch is the input offset current, which can only be minimized when good layout techniques for the current mirrors ($M_2$, $M_4$, $M_8$ and $M_{12}$) and the current sources ($M_5$, $M_6$, $M_{11}$ and $M_{13}$) can be achieved. A fully differential input transconductor is realized using two transconductors as shown in Figure 3.4(b).




(a)




(b)

**Figure 3.4:** Opamp design using linear transconductor with resistor input.

The outputs of the transconductors are cross-coupled in order to make the output current unchanged when both input voltages of the transconductors are equal. Therefore, the common-mode input signal is rejected and a good common-mode rejection ratio (CMRR) can be achieved. In Figure 3.4(b), the transconductor current outputs are converted to voltage using a transimpedance amplifier. The output voltage is given:

$$V_{out} = R_1 \cdot g_m (v_{ip} - v_{in}) \tag{3.8}$$

Since the value of $g_m$ is inversely proportional to the resistor R (shown in Figure 3.4(a)), the accuracy of the amplifier gain is mainly determined by resistor matching. Slew rate and settling time for 0.1% accuracy were measured to be approximately 2.24 V/μs and 1 μs respectively when implemented in 1.2 μm CMOS process [14]. When connected as a unity-gain noninverting buffer, a THD of –72 dB was measured for a 10kHz 0.6 $V_{p-p}$ sine-wave input. The CMRR was measured to be greater than 43 dB.

Floating-gate MOS transistor have been used in digital EPROM or EEPROM for decades, but they are not so widely used in analog circuits. In fact, only few results have been published such as, floating-gate CMOS analog trimming circuit in standard process [23], D/A converters [24], etc. An exciting property of floating-gate MOSFET is that the electric isolation from the floating-gate to other nodes is so ideal that the electrical charge can stay there for several years with a variation of less than 2 % at room temperature. Floating-gate MOS differential pair has been used to obtain a rail-to-rail input CM range [16], as illustrated in Figure 3.5(a). In order to allow rail-to-rail input operation, the opamp input signals are attenuated and taken to a potential very close to

one of the supply rail. This is done by means of a capacitive divider implemented with multiple-input floating-gate transistors (MIFGTs).

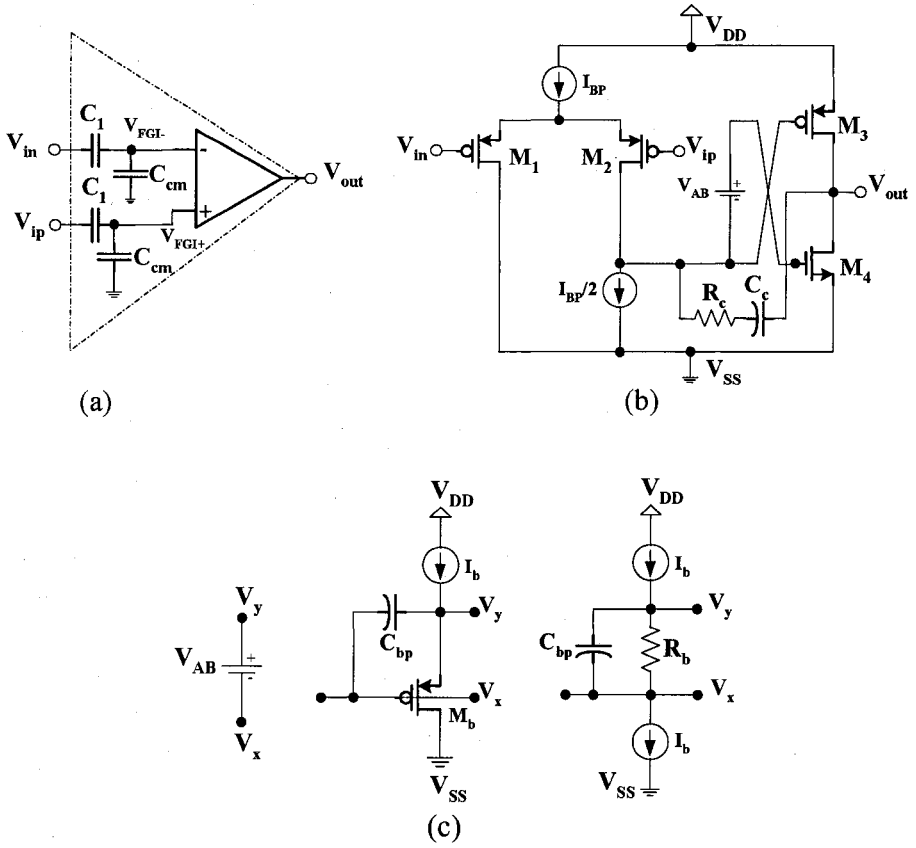



**Figure 3.5:** Low-voltage opamp using floating-gate transistors: (a) basic scheme, (b) two-stage single ended scheme, (c) two possible implementations of the floating battery.

To this purpose, the floating gate of each MIFGT is biased by connecting one of its inputs to one supply rail (ground in Figure 3.5(a)), while the other input terminals are used to apply signals.

For very low-voltage operation, the capacitor connected to the supply rail needs to be larger than the capacitors connected to the signal. This approach has the following advantages:

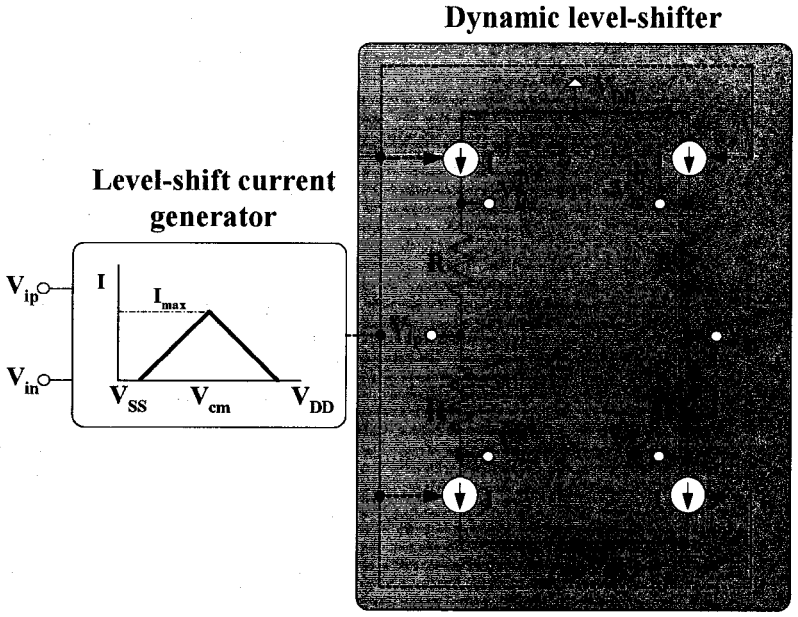
- As a single differential-pair is used, a constant $g_m$ is obtained over the full input range and there is no CMRR degradation due to the operation of two complementary differential pairs;
- Capacitive dividers do not introduce dc input impedance degradation; neither do they load the input source or the output terminals of the opamps;
- No additional noise is introduced by the capacitive elements;
- This scheme allows easy implementation of linear weighted addition of several signals, given that this is a basic characteristic of MIFGT circuits, with the weight determined by input capacitor ratios.

The price paid for low-voltage operation using MIFGTs is an effective reduction in the transconductance of the input stage, and therefore, in the opamp dynamic range and gain-bandwidth product. Figure 3.5(b) is the basic two-stage architecture of the low-voltage opamp. The first stage is the aforementioned differential pair with MIFGT (depicted as conventional MOS) and the second stage is a low-voltage class-AB CMOS inverter modified by the addition of a floating biasing battery with value $V_{AB}$ located between the gates of the inverter's transistors. This battery has a negative polarity,

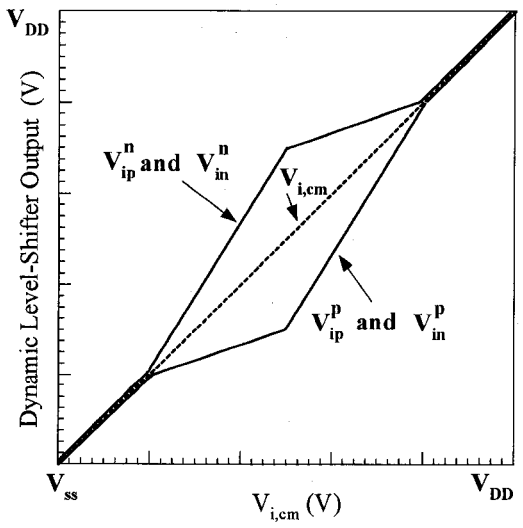
which allows the supply $V_{DD}$ to be reduced to a value close to one transistor's threshold voltage. Figure 3.5(c) shows two implementations of the floating battery $V_{AB}$. The first one (on the left) uses a transistor $M_b$ biased with a small current $I_b$, and the second case (on the right) uses a resistor $R_b$ instead of $M_b$. This low-voltage class-AB output stage provides the circuit with very attractive characteristics such as rail-to-rail output, low quiescent power dissipation and high slew rate, since the maximum load current can be much greater than the quiescent current (although, for small load capacitance, the slew rate is limited by the tail current of the input differential pair and the compensation capacitor $C_C$). Other class-AB topologies suitable for low-voltage (1-V or less) such as those described in [25]-[27] can also be used. The simulated THD for a 150 KHz sinusoidal input was 0.09 % and the equivalent input noise in the bandwidth of the circuit was 127 μ V while the input noise power density was found to 48 nV/$\sqrt{Hz}$ in [15]. Even if the technique has been applied in a double poly CMOS technology, it can be extended to digital CMOS technology using the method described in [23] related to the implementation of floating-gate transistors in digital technology.

Resistive dynamic level shift [17]-[18] as depicted in Figure 3.6, has been used to realize near rail-to-rail CM input swing. When the supply voltage drops to below ($2V_{th}$ + $4V_{DS,sat}$), the n-p complementary stage does not provide a rail-to-rail CM input range. The problem can be solved if four level shifters are inserted between the direct inputs and the gates of the input stage transistors (Figure 3.6(a)). Because active components cease to operate under small voltage headroom, we have to resort to passive components, i.e. resistors, to realize the level shifters. The bipolar version of the concept

was proposed in [17], and a 1-V near rail-to-rail input and output bipolar opamp was successfully implemented.




(a)



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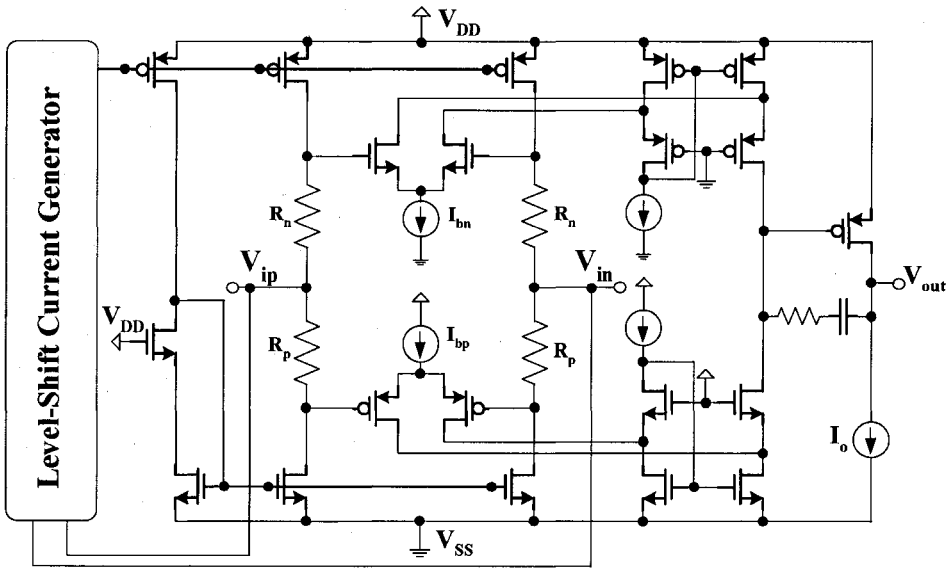


(c)

**Figure 3.6:** Low-voltage rail-to-rail CMOS opamp using continuous-time dynamic level shifter: (a) conceptual schematic, (b) common-mode components versus input CM $V_{i,cm}$, (c) 1-V rail-to-rail complementary input stage.

As illustrated in Figure 3.6(a), the input voltage ($V_{ip}$ or $V_{in}$) is applied to the pMOS ($V_{ip}^{p}$ or $V_{in}^{p}$) and the nMOS ($V_{ip}^{n}$ or $V_{in}^{n}$) differential pairs through voltage level shift resistors R. The level shift current and voltage, which are shaped through a feedback network (not shown in the Figure), change with the common-mode input voltage as shown in Figure 3.6(b). Figure 3.6(b) also illustrates the curves of the base voltage of the input transistors versus CM input voltage $V_{i,cm}$

A 1-V rail-to-rail CMOS opamp was implemented by Duque-Carrillo et. al [18] and shown in Figure 3.6(c). Details of the level shift current characteristic are well described in [18] with its CMOS implementation. The input stage does not present a constant $g_m$ over the whole CM range due to its simple design. Another opamp with a rail-to-rail CMR for a 1-V operation was implemented in the same paper [18] only with a pMOS differential pair. Its distortion performance is much better than in the previous case (Figure 3.6c), as a consequence of only using one differential pair, and therefore, no problem with the offset voltage variation exists. The problem of the resistor area is more critical in the approach represented in Figure 3.6(c).

It is clear that 1 V opamps can be implemented by attenuating the input signal using capacitive, resistive divider or level shifter. The resistive ones ([13], [17]-[18]), however exhibit a much larger input current and much more input noise. This is why they are not often used.

### 2. Bulk driven and current driven bulk MOSFET based opamp method

Low-voltage rail-to-rail CM input swing can also be achieved using the bulk-driven differential pair technique. The original purpose of this technique was to yield a small $g_m$ and to improve linearity [19]. In [20], a 1-V opamp was designed using the depletion characteristic of the bulk-driven transistors to have a rail-to-rail CM range and to meet the low-voltage requirement. The full opamp circuit implementation is shown in Figure 3.7. This type of opamp requires low supply, about ($V_{GS}$ + $V_{SD,sat}$). Its shortcoming is that the transconductance value changes dramatically (about 2 times)

with the CM input voltage. The equivalent input referred noise of a bulk-driven MOS amplifier is larger than the conventional gate-driven MOS amplifier because of its small transconductance. It has the proneness to turn on the parasitic bipolar transistors, which may result in a latch-up problem.

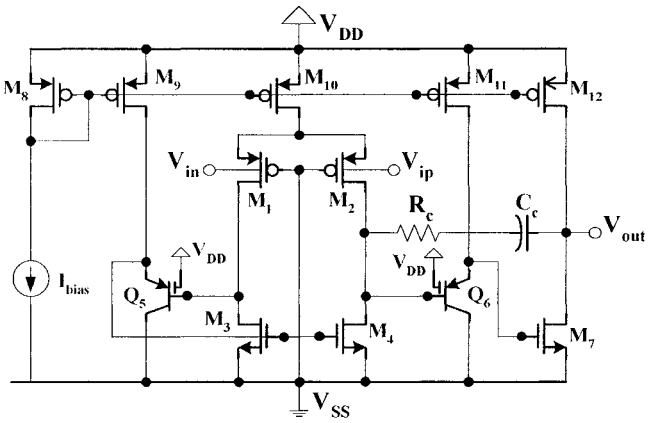


**Figure 3.7:** 1-V rail-to-rail bulk driven CMOS opamp

The threshold voltage of a MOS transistor as a function of bulk-source voltage $V_{BS}$ is given by Equation (3.9):

$$V_{th} = V_{th0} + \gamma\left(\sqrt{|2\cdot\phi_F - V_{BS}|} - \sqrt{|2\cdot\phi_F|}\right) \tag{3.9}$$

where $V_{th0}$ is zero bias threshold voltage, $\gamma$ the bulk effect factor and $\phi_F$ the Fermi potential. For a p-channel transistor, $2\cdot\phi_F \approx$ -0.7 V, $\gamma \approx$ -0.5 $\sqrt{V}$ and $V_{th0} \approx$ -0.6 V, typically, a bulk bias $V_{BS}$ is normally greater than 0, which leads to an increase of the threshold voltage. However, by biasing $V_{BS} < 0$ V, we can actually decrease the threshold voltage [28]. Thus, to reduce the threshold voltage as much as possible, the device is bulk biased as high as possible. This will, however, forward bias the bulk-

source diode, i.e., the base-emitter diode of the associated parasitic bipolar transistor, thereby turning on the BJT. $|V_{BS}|$ is limited by how much current the new BJT can tolerate. This is the basic idea of the current driven bulk (CDB) circuit technique. This method has been used to implement a 1-V CMOS OTA [21] as shown in Figure 3.8.

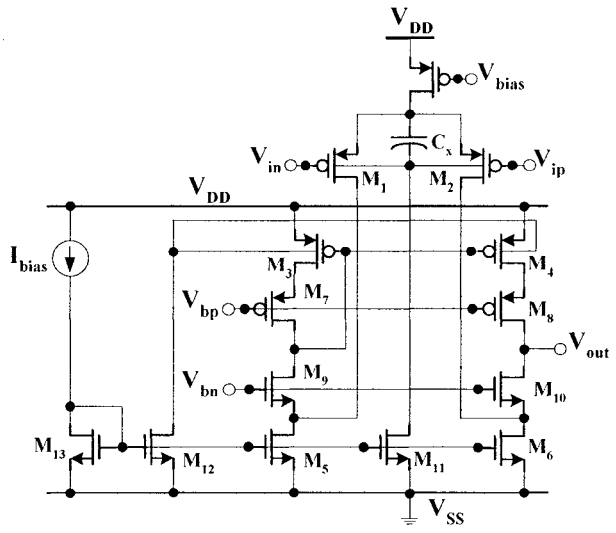


**Figure 3.8:** 1-V CDB folded cascode OTA.

The threshold voltage of the differential pair ($M_1$-$M_2$) is reduced and thus leads to a direct improvement of the CM input range. Note that, only one current source has been used for the common bulk terminal in the pair (rather than individual current drives for each transistor); otherwise, mismatch problems in the pair will appear. Any noise injected because of the current drive will enter the amplifier as a common-mode signal and thus will be rejected. Operation of this circuit down to 0.7 V has been reported. Current driving the bulk introduces unsuited effects in the resulting devices. The first obvious one is the parallel connection of the BJT emitter/collector with the MOS

source/drain; this must lower the device output impedance. If the BJT emitter current is much smaller than the MOS source current, the effect is negligible. Noise from the BJT would also enter the circuit, but again, if the current in this device is low, we would expect only a small amount of added noise. It's evident that the drain-bulk capacitance has a major impact on high frequency circuit performance. Several ways can be used to cancel its effect.

A similar technique has been used by Annema [29] to build an opamp for low-voltage bandgap reference voltage circuit (Figure 3.9). A dynamic threshold MOS (DTMOS) transistor [30] is used instead. The input driven differential pair consists of DTMOS $M_1$-$M_2$. The device is basically a MOS transistor with an interconnected well and gate.

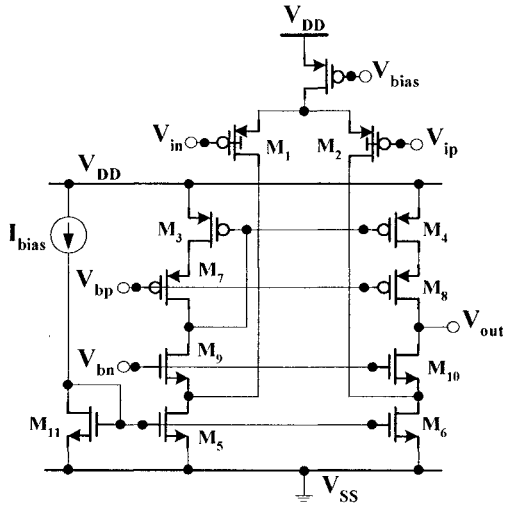


**Figure 3.9:** Low-voltage opamp based on DTMOS: simple implementation.

Only p-type DTMOS can be used due to the fact that their n-well can be controlled in standard digital CMOS technology. The operation of the DTMOS is similar to weak-inversion pMOS operation and has similarities with bipolar operation in, for example, lateral pnp's. The spread and matching of the DTMOS is caused by the same mechanism that leads to $V_{th}$ variations in MOS transistors such as well-doped fluctuations and oxide thickness variations [31]. However, it appears from both device simulations [29] and device measurements that the $V_{GS}$ variations in DTMOS are only about half the value of the $V_{th}$ variations in an equally large pMOS transistor (with interconnected well-source) operated at the same current. Hence the matching of two DTMOS is about twice as good as the matching between the same devices operated as (source-well-interconnected) pMOS transistors at the same current. Also the batch-to-batch variations (the spread in $V_{GS}$ and in $V_{th}$) of DTMOS is about half of the value of their pMOS counterparts.

The design of the folded cascode rail-to-rail input stage is not different from a classical folded cascode input stage with respect to gain, noise and frequency behavior. The problem of CMOS opamp circuit sizing is covered by Mandal [32]. Given a circuit and its performance specifications, the described approach, automatically determines the device sizes in order to meet the given performance specifications while minimizing a cost function, such as weighted sum of the active area and power dissipation. The approach is based on the observation that the first order behavior of a MOS transistor in the saturation region is such that the cost and the constraint functions for the optimization problem can be modeled as polynomial in the design variables.

## B. Analog CMOS switches

Analog switches are used in various circuits such as: multiplexers, sample-and-hold (S/H) circuits, analog-to-digital converters (ADCs), digital-to-analog converters (DACs), and in particular in discrete-time analog systems such as switched-capacitor (SC) and switched-current (SI) building blocks.

One of the main characteristics of the MOS transistors is the switching feature. Drain and source terminals are the two switch terminals and the gate (and sometimes the bulk) is used to control the conductivity. Ideally, the switch in the on state acts as a fixed linear conductance $g_{ds}$. In practice, the conductance is strongly signal-dependent. The switch conductivity depends not on the absolute potential of the control terminals, but on their potential relative to the others. Also the conductance through the whole range of input is not constant, and depends on the supply voltage, which becomes extremely low and therefore leading to a dead band conduction region. To ensure rail-to-rail switching operations control, signals exceeding the supply voltage range are required. This is known as bootstrapped switching technique [33].

A general block diagram of the bootstrapped switch is shown in Figure 3.10. It consists of three main elements: the pass-transistor (nMOS, pMOS or both types), a control signal generator and, finally, a clock booster. The control circuit generates a signal linearly related to the input signal. The purpose of the clock booster is to generate a clock signal over and above the supply voltage. For the purpose of sampling a

continuous-time signal, Brooks proposed a bootstrapping technique [33], where the gate-to-channel voltage is almost constant in sampling phase.

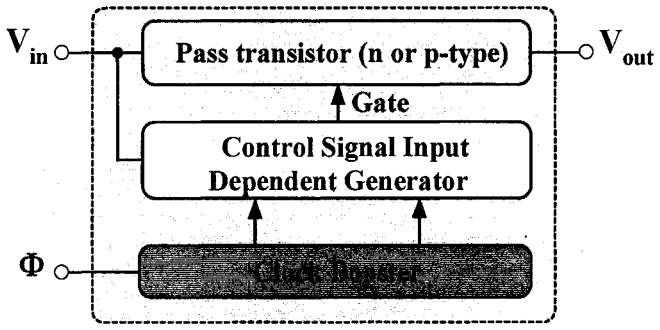


**Figure 3.10:** Block diagram of bootstrapping switch.

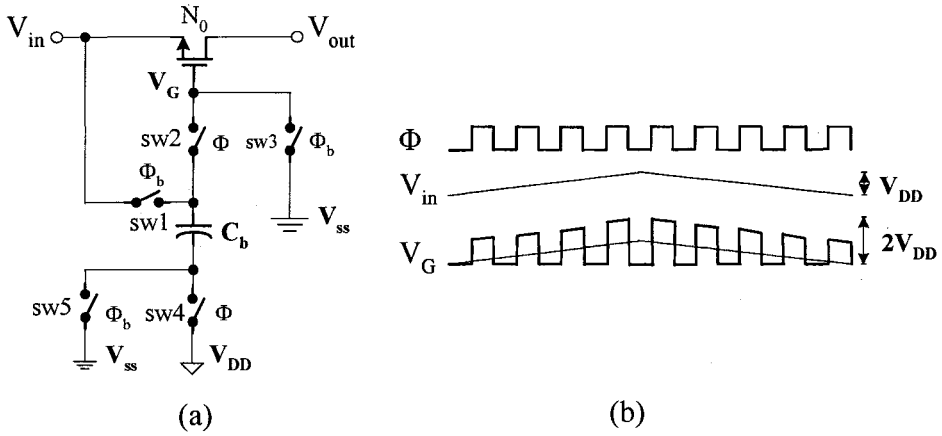


**Figure 3.11:** Bootstrapped-clock boosted input switch: principle of operation, (b) interval node voltage variation.

The input dependent control signal part is shown in Figure 3.11 with the n-type pass transistor $N_0$. Neglecting the body-effect, the switch's conductance will be signal

independent and the main switch element gate oxide will not be subject to unacceptable large electric fields when $t_{ox}$ is high. In reality, the conductance is given by:

$$g_{ds} = \left(\mu C_{ox}\frac{W}{L}\right)_n \left[V_{DD} - V_{th,n} - \gamma_n \cdot \left(\sqrt{2\cdot\phi_f + V_{in}} - \sqrt{2\cdot\phi_f}\right)\right] \qquad (3.10)$$

and cannot be compensated for the body-effect (n-type devices share the same substrate or bulk which is connected to $V_{ss}$).

Rebeschini has proposed an improved concept (which does not require the continuous-time signal to be highly oversampled) in [34] and is shown in Figure 3.12.

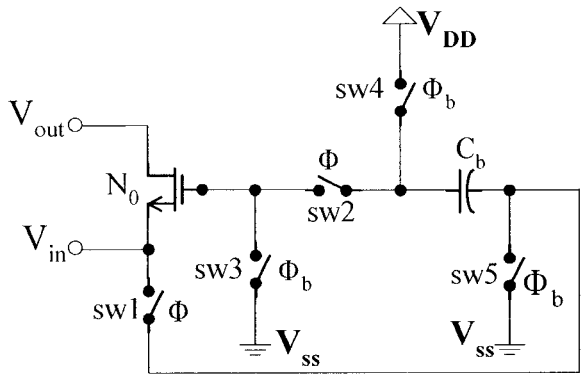


**Figure 3.12:** Modified bootstrap switch principle.

The main difference is that the bootstrap capacitor $C_b$ is connected between the drain and gate during the sampling mode. Jesper [35] has proposed a low-voltage, low-stress circuit implementation of this concept and the control dependent input signal part is shown in Figure 3.13 with the pass transistor $N_0$. Abo [36] performed a similar implementation at the same time.

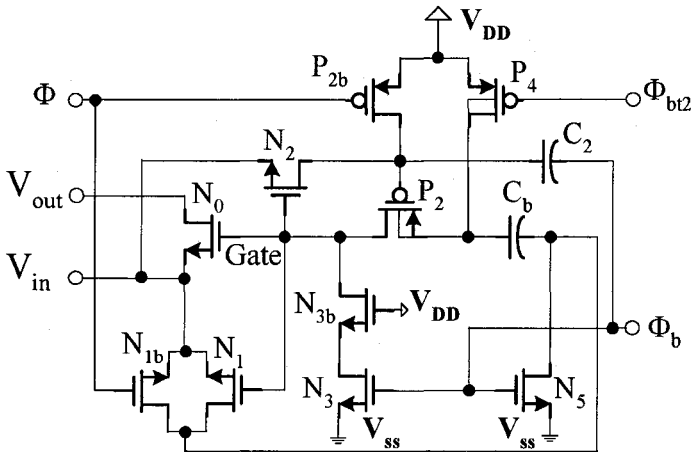


**Figure 3.13:** Bootstrapped nMOS switch.

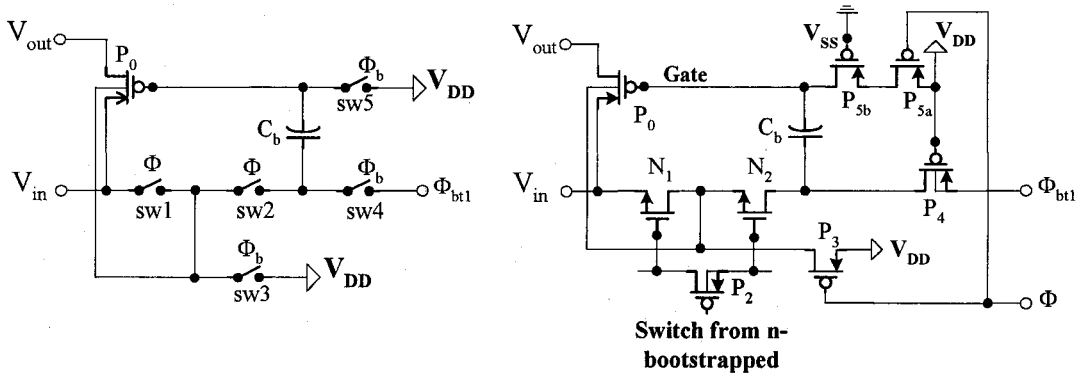


**Figure 3.14:** Low-Voltage body-effect compensated pMOS switch: (a) principle of operation, (b) MOS circuit implementation.

To compensate for body-effect at low voltage, the concept has been modified by Jesper [35] and is shown in Figure 3.14(a) with its circuit implementation of Figure

3.14(b). The bootstrap capacitor is connected directly to the gate terminal of $P_0$. Transistor $P_0$ is compensated for the body effect by connecting the bulk terminal to $V_{in}$ in the on state. Switches sw2 and sw3 can, in principle, be a short and open circuit respectively, but they could be real switches to avoid loading the charge pump by the well in which $P_0$ is connected. The gates of transistor $N_1$ and $N_2$ (Figure 3.14(b)) are respectively controlled by the drain and source terminals of transistor $P_2$ of Figure 3.13. A simpler implementation has been proposed in [12] and shown in Figure 3.15(a).

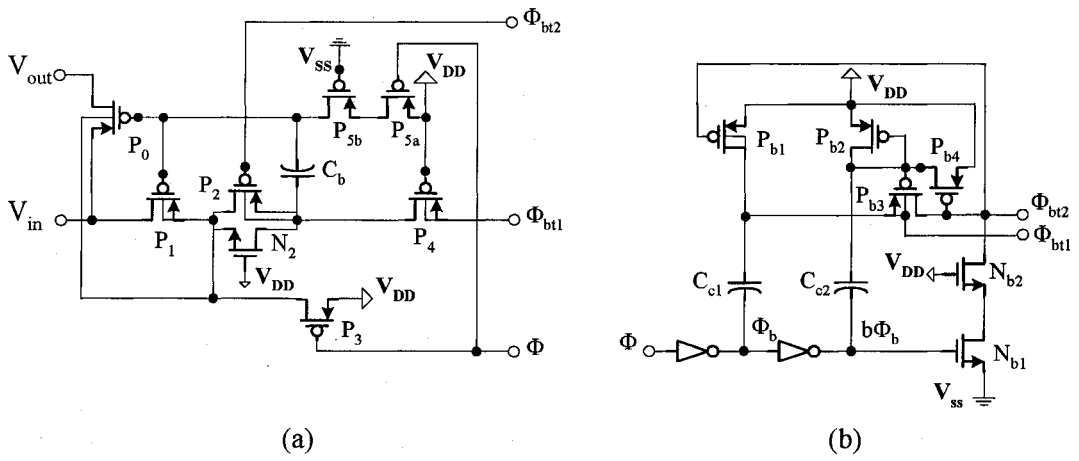


**Figure 3.15:** (a) Simple low-voltage pMOS bootstrapped switch, (b) pMOS clock booster circuit.

The circuit makes use of a novel low-voltage pMOS clock booster circuit (Figure 3.15(b)). Feedback transistor $P_{b4}$ keeps the gate-drain voltage of transistor $P_{b3}$ to a reasonably low level and is subjected to a maximum source-gate voltage of $V_{DD} + |V_{th,p}|$, which is acceptable in most processes. A wide variety implementation of the bootstrap

switch concept exists in the literature [36]-[40]. The most recommended for low-voltage applications are those of [36] and [12] due to their simplicity and built-in body-effect compensation.

## III. CAPACITOR IMPLEMENTATION IN STANDARD CMOS TECHNOLOGY

Capacitors are one of the crucial elements extensively used in the integrated circuits such as data converters, S/H, SC circuits, radio frequency (RF) oscillators and mixers. Capacitors can occupy considerable area; therefore, an area-efficient capacitor is highly desirable. The problem is more pronounced in modern technologies where the vertical spacing of the metal does not down scale well.

Four types of capacitors have been commonly used in IC design: gate capacitors, junction capacitors, conventional metal-to-metal/poly capacitors, and thin-insulator capacitors.

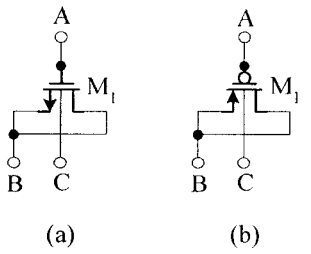


**Figure 3.16:** MOS gate capacitors: (a) nMOS; (b) pMOS

Gate capacitors (Figure 3.16) have high density (high capacitance per unit area), are always available in any process, but are nonlinear and require a dc bias voltage to operate. Due to the thin gate oxide, gate capacitors have a low breakdown voltage. They

also have a medium quality factor Q. Junction capacitors suffer from some of the above problems as well. They are highly nonlinear, and they also need a dc bias voltage. In addition, their sensitivity to process variations, poor quality factor and large temperature coefficient limit their use in many applications. Metal-to-metal and metal-to-poly capacitors, on the other hand, are linear and have high Q. They also exhibit very small temperature variations. Unfortunately, the density of a traditional metal-to-metal capacitor is very low due to the relatively thick interlevel oxide layers. The problem becomes more severe with scaled technologies since the vertical spacing of the metal layers stays relatively constant. As a result, standard parallel-plate capacitors consume a larger percentage of the die as technology down scales. There has been a recent growth in the use of thin-insulator capacitors in IC applications. Double-poly capacitors and metal-insulator-metal (MIM) capacitors use a thin oxide to achieve high density [41]. The capacitance density is much higher than the density of a standard metal-to-metal capacitor, but it is lower than the gate capacitor built in the same technology. The need for additional masks and process steps makes these capacitors more expensive comparing to other types of capacitors. Double-poly and MIM capacitors are highly linear and have high quality factors, but due to the cost overhead, they are generally not available in standard digital processes.

Three techniques for the implementation of capacitors in standard digital processes will be covered in the next section. The first is related to the lateral flux capacitors [42]-[43], whereas the two others techniques are related to MOS gate-capacitance [44] and junction capacitors [45].

## A. Lateral flux capacitors

Figure 3.17(a) shows a lateral flux capacitor. In this capacitor, the two terminals of the devices are built using a single layer of metal, unlike a vertical flux capacitor, where two different metal layers must be used. As process technologies continue to scale down, lateral fringing becomes more important. The lateral spacing of the metal layers (s) shrinks with scaling, while the thickness of the metal layers (t) and the vertical spacing of the metal layers ($t_m$) stay relatively constant. This means that, structures utilizing lateral flux enjoy a significant improvement with process scaling, unlike conventional structures that depend on vertical flux. A scaled lateral flux capacitor is shown in Figure 3.17(b), it is obvious that the capacitor is larger than the one of Figure 3.17(a).

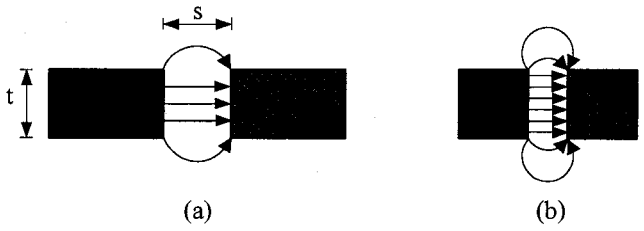


**Figure 3.17:** Effect of scaling on lateral flux capacitors: (a) before scaling and (b) after scaling.

Lateral flux can be used to increase the total capacitance in a given area. Figure 3.18(a) is standard parallel-plate capacitor. In Figure 3.18(b), the plates are broken into cross-connected sections [40]. A higher capacitance density can be achieved by using

lateral flux capacitor as well as vertical flux. The idea can be extended to multiple metal layers as well.

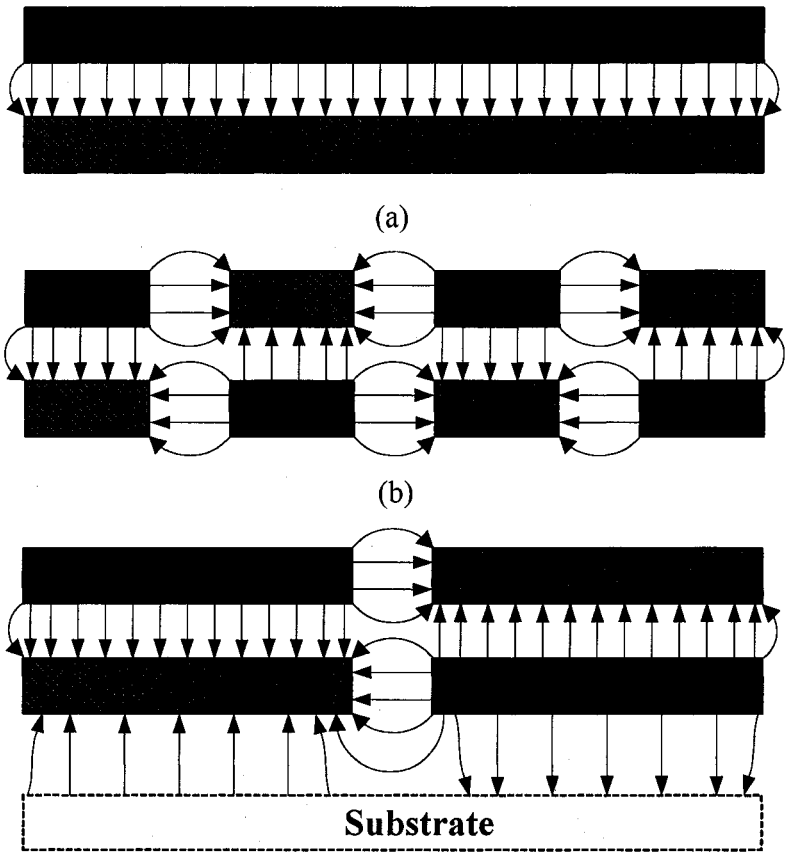


**Figure 3.18:** Vertical versus lateral flux: (a) a standard parallel-plate structure, (b) cross-connected metal layers and (c) reduction of the bottom-plate parasitic capacitance.

One advantage of using lateral flux capacitors is the reduction of the bottom-plate capacitance. This reduction is due to two reasons. First, the higher density results in a smaller area [43]. Second, some of the fields lines originating from the one of the bottom

plates terminate on the adjacent plate instead of the substrate, which further reduces the bottom-plate capacitance as shown in Figure 3.18(c). Because of this property, some portion of the parasitic bottom-plate capacitor is converted into more useful plate-to-plate capacitor.

In current IC technologies, there is usually tighter control over the lateral spacing of metal layers compared to the vertical thickness of oxide layers, from wafer to wafer and across the same wafer. Lateral flux capacitors shift the burden of matching away from the oxide thickness to the lithography. In other words, by using lateral flux, matching characteristics can improve. Furthermore, the pseudorandom nature of the structure can also compensate, to some extent, for the effects of non-uniformity of the etching process. To achieve accurate ratio matching, multiple copies of a unit cell should be used.

Another simple way of increasing lateral flux's capacitance density is to use the interdigitated capacitor depicted in Figure 3.19. The interdigitated structures are more vulnerable to non-uniformity of the etching process. However, the relative simplicity of interdigitated capacitor does make it useful in some applications. An empirical formula for estimating the lateral flux capacitor is given in [46], whereas its theoretical limits for density are derived in [47]. Capacitance structure based on [43] achieves a factor of 3.4 capacitance density improvement over the standard horizontal parallel plate (HPP) using only two metal layers but for equal capacitance values demonstrate a higher self-resonance frequency than the HPP structure [47]. In terms of series resistances, [43] capacitance structure has a series resistance $r_s$ of 0.57 Ω comparable to $r_s$ of 1.1 Ω for

the HPP. An implemented capacitors using 5-metal layer in a purely digital CMOS 7-metal layer process technology ($L_{min} = W_{min} = 0.24$ μm, $t_{ox} = 0.7$ μm and a metal layer thickness $t_m = 0.53$ μm) exhibits a density of 1512 aF/ $\mu m^2$.

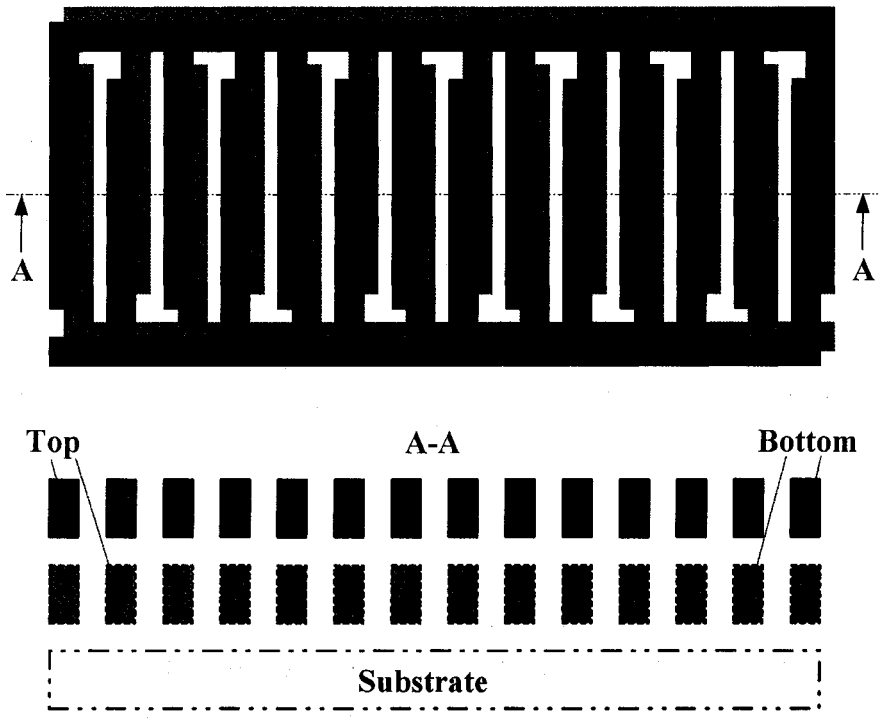


**Figure 3.19:** An interdigitated capacitor.

## B. MOS transistors as capacitors

Recently published method for implementing a capacitor using a regular MOS is shown in Figure 3.20 [44]. MOS devices are laid out either adjacent or interdigitated in the same n-well (pMOS case of Figure 3.20(b)). The purpose of the resistor $R_{big}$ is to bias the n-well and p-substrate for the pMOS and nMOS devices respectively.

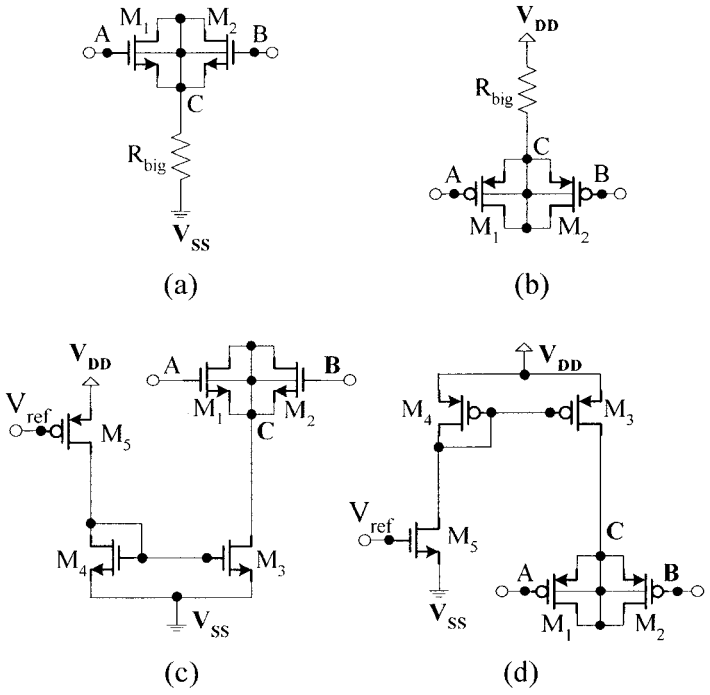


**Figure 3.20:** A floating MOS capacitor implementation: (a) nMOS, (b) pMOS and its circuit realization (c) nMOS, (d) pMOS.

A circuit realization of these capacitors is also shown in Figure 3.20(c-d). However, in standard digital processes, only the pMOS implementation (Figure 3.20 (d)) is possible. Circuit realization based on Figure 3.20(c) is also possible in standard digital processes. In this case the bulk or substrate connection to source has to be removed and thus, making the implementation more susceptible to noise from adjacent circuitry. Transistor $M_3$ is operating within its linear regime, it acts as a high-impedance resistor to ground, biasing the bias terminal C to ground. At this point, capacitive structure formed by $M_1$-$M_2$, provides constant capacitance as long as both devices $M_1$ and $M_2$ are

operating in their respective saturation regimes. Therefore, transistor $M_1$ and $M_2$ must each satisfy the relationship:

$$V_{A,B} - V_C \leq V_{th,p} \tag{3.11}$$

where $V_C$ is the bias voltage applied to bias terminal C, and $V_{th,p}$ and $V_{A,B}$ are the threshold voltage and the gate terminal voltage, respectively, of either transistor $M_1$ or $M_2$. $V_C$, which is determined by current generator and current mirror, is at the power supply $V_{DD}$, so the capacitive structure provides constant capacitance as long as the gate terminal voltages of transistor $M_1$ and $M_2$ are both in the range between $V_{SS}$ and $V_{DD} + V_{th,p}$. The external reference voltage $V_{ref}$ sets this current. The biasing circuit could be implemented in any manner that provides a high-impedance output or a low current leakage path, such as a transistor network. Finally, any circuit for a current source, such as cascode current source, and for a current mirror, such as Wilson current mirror, could be used instead of the previously described circuit. Assuming both transistors ($M_1$ et $M_2$) operate in saturation region, the effective capacitance $C_{AB}$, of this structure, is half of the gate terminal capacitance. Its typical density is 2.81 fF/μm in a standard 0.18 μm digital CMOS process.

Another method for implementing high linear MOS capacitor is proposed by Tille et. al [45]. A series nonlinear compensation circuit using well biased is adopted (Figure 3.21(a)). Well biasing keeps the MOS capacitors in a broad depletion region, producing an extension of the usable voltage range and a first order cancellation of the nonlinear effect. The series compensation is obtained by connecting the gate nodes of two MOS capacitors, and the usable capacitance is available between the bulk nodes A and B.

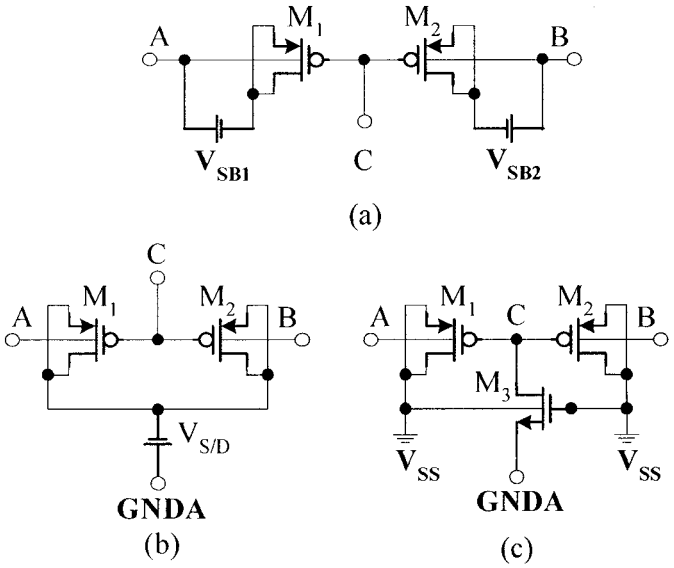


**Figure 3.21:** Series compensation MOS capacitors using well-biased MOSFETs in depletion mode: (a) principle of operation, (b) circuit realization without floating dc voltage source, (c) circuit realization with fixed well bias and a high resistance element.

To realize floating capacitors, p-channel MOSFETs embedded in a separate n-wells are chosen. The drain and source contacts of each of the p-channel MOSFETs $M_1$ and $M_2$ are shorted. The dc voltages $V_{SB1}$ and $V_{SB2}$ are the well bias voltages between drain/source and the bulk nodes A and B, respectively. If MOS capacitors of equal area are used, the substrate bias voltages $V_{SB1}$ and $V_{SB2}$ should be of the same value to guarantee the optimal nonlinearity compensation effect. For the capacitor expression derivation, it is assumed that the capacitance $C_{GB1}$ and $C_{GB2}$ of the MOS capacitors $M_1$ and $M_2$ are equal and gate node C is not charged. Hence, the potential at node C varies

at the middle between the potential of nodes A and B, respectively. Then, the total capacitance $C_{serD}$ of a series compensated depletion-mode MOS capacitor is the series capacitance of both capacitances $C_{GB1}$ and $C_{GB2}$. A close formula for the resulting capacitance is given in [45] as:

$$C_{SerD} = C_{ox}\left(\sqrt{1+4\frac{|V_{GB1}+V_{FB}|}{\gamma^2}}+\sqrt{1+4\frac{|V_{GB2}-V_{FB}|}{\gamma^2}}\right)^{-1} \tag{3.12}$$

where $C_{ox}$ is the gate-oxide capacitance, $\gamma$ the body-effect coefficient and $V_{FB}$ the flat-band voltage.

In the circuit implementation of Figure 3.21(b), the shorted drain and source nodes of both MOSFETs $M_1$ and $M_2$ are connected together and then this node is biased negative relative to analog ground. Note that the bias voltage $V_{S/D}$ must not become larger than the bulk voltages otherwise the pn junctions between drain/source and n-well of the MOSFETs $M_1$ and $M_2$ turn on. The best way to prevent this is to connect the shorted drain/source nodes to $V_{SS}$, which simplifies the implementation. To obtain a high resistance element on node C in order to prevent a gate charging, a n-channel MOSFET $M_3$, operated in the substhreshold region is used (Figure 3.21(c)). Finally, to avoid significant parasitic capacitances, the area of the MOSFET $M_3$ should be small relative to the areas of the MOSFETs $M_1$ and $M_2$. Series compensation capacitor combines high linearity with moderate area efficient. A typical density of 0.4 fF/$\mu m^2$ has been reported for a purely digital 0.18 μm CMOS process [4]. A 0.0138 % nonlinearity

is obtained for a signal amplitude of 0.21 $V_{p-p}$ at a common-mode offset voltage of 105 mV.

**Table 3.3:** Comparison of capacitors implementation in standard CMOS processes.

| | Akcasu [43] | Hariton [44] | Till et. al [45] |
|---|---|---|---|
| **Method** | Fringing (Metal-Metal) | Floating-gate MOS | Depletion-mode MOS |
| Density | 1.5 fF/$\mu m^2$ | 2.8 fF/$\mu m^2$ | 0.4 fF/$\mu m^2$ |
| Parasitic | Small | Negligible | Negligible |
| Linearity | High | High | 0.013 % 0.21 $V_{p-p}$ for CM around 0.15 V |
| Input Common Range | Limited by the breakdown voltage | $V_{SS}$ to $V_{DD}$ - $\|V_{th,p}\|$ | Varies with Analog ground |

In analog integrated circuits, techniques to ensure the matching of this capacitor structure as well as good layout practice are described in [48], [49]. We summarize in Table 3.3, the state-of-the-art capacitor implementation methods. As MOS processes continues to downscaling, the fringing-effects based capacitor implementation [43] will gain more interest compared to classical parallel-plate capacitor. The floating-gate MOS based capacitors [44] exhibits a high area efficiency and linearity compared to the series compensation [4]-[45].

## IV. CONCLUSION

Various topologies related to low-voltage analog building blocks circuit design were reviewed, ranging from low-voltage opamp to the implementation of CMOS analog switch and capacitors to name just a few examples. Applications of the circuit extend

from sample-data systems to switched-capacitor filter and rail-to-rail data converters to just name a few. These buildings blocks are useful in designing low-voltage CMOS circuits and systems in standard digital processes.

## ACKNOWLEDGMENTS

The authors would like to acknowledge the financial support from the Natural Sciences and Engineering Research Council of Canada (NSERC) and Micronet.

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Low-voltage design remains a concern as technology continues to scale downward. Supply voltage decreases as feature sizes shrink. Analog buildings blocks, ranging from operational amplifiers, analog CMOS switches to bandgap reference voltage, which follow this trend have been described above. Challenges involved in the implementation of capacitors are covered with some approaches to overcome these limitations.

The next chapter will focus on design strategy for the implementation of analog MOS as a sample-and-hold circuit operating at 1-V supply voltage and below.

# *Chapter 4*

# *RELIABLE IMPLEMENTATION OF A MOS SWITCH-BASED SAMPLE-AND-HOLD CIRCUIT*

The main function of a sample-and-hold circuit (S/H) is to take samples of its input signal and hold these samples on its output for some period of time. Typically, the samples are taken at uniform time intervals; thus, the sampling rate (or clock rate) of the circuit can be determined. Various methods can be used to realize this function. The purpose of this chapter is to describe the operation and design methodologies of analog switches used as a sample-and-hold circuit in submicron processes.

## 4.1 Analog CMOS switches

A fundamental component of any dynamic circuit (analog or digital) is the switch (Figure 4.1). An important attribute of the switch in CMOS is that under DC conditions, the gate of the MOSFET does not draw a current. Therefore, neglecting capacitances from the gate to drain/source, we find that the gate control signal does not interfere with the information being passed through the switch.

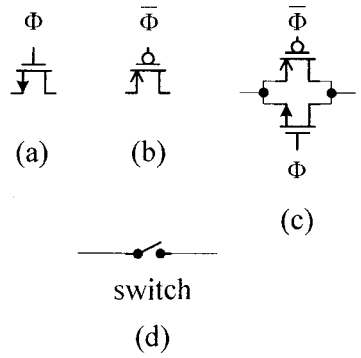


**Figure 4.1:** MOSFETs used as switches: (a) nMOS, (b) pMOS, (c) Transmission gate, (d) symbolic representation.

Plot in Figure 2.3 (Chapter 2) shows the small signal conductance of the switches of Figure 4.1 against source voltage. The benefits of using the CMOS transmission gate (TG) are seen from this figure, namely, lower overall conductance. Another benefit of using CMOS TG is that it can pass logic high or logic low without a threshold voltage drop. The larger voltage a n-channel switch can pass is $V_{DD}$-$V_{th,n}$, while the lowest voltage a p-channel switch can pass is $|V_{th,\,p}|$.

While MOS switches may offer substantial benefits, they are not without some detraction. Two non-ideal effects typically associated with these switches may ultimately limit the use of MOS switches in some applications (particularly sampled-data circuits such as data converters). These two effects are known as charge injection and clock feedthrough [SHE84], [SHI87], [WIL85] and can cause error voltage and thus introducing significant error in analog circuits employing switched capacitors. Many circuit design techniques have been developed to reduce this error voltage. These techniques result in increased complexity while lowering the operating frequency,

without nulling its effects in most cases. Estimating this error prior to simulation would aid in the design process by relating the design parameters such as source resistance, device size, load capacitance, and the control signal fall time to the error. This has been done by Sheu [SHE84]. Although analytical expressions to estimate this error have been developed, they fail to incorporate the effect of source resistance in the circuit and are complex to use.

The main objective of the following section is to describe the design process, silicon implementation and experimental results of the proposed deep submicron analog switch.

## 4.2 Low-Voltage Analog Switch in Deep Submicron CMOS: Design Technique and Subsequent Measurement (Journal paper no. 2)

In this paper, we introduce a simple and easier way of solving all these effects in [FAY03b]. Design techniques for constant ON-resistance of CMOS analog switches in deep submicron standard process have been introduced. Methods to reduce the clock feedthrough and charge injection have been covered. The heart of this design is an ultra low-voltage clock signal doubler. This circuit allows the generation of a control signal, which is input dependent, to ensure a constant switch's ON-resistance with a constant charge injection. Doubling voltage on ultra-thin oxide device can introduce some reliability problem. In this paper, critical devices have been pointed out from the circuit and design equations have been given. We also covered physical layout and design guidelines to ensure robustness and reliability of the design.

# Low-Voltage Analog Switch in Deep Submicron CMOS: Design Technique and Subsequent Measurement

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Journal: IEEE Transactions on Circuits and Systems II

Status: Submitted on February 2003

**Abstract**

This paper concerns the design, implementation and subsequent experimental validation of a low-voltage analog CMOS switch based on gated bootstrapped method. The main part of the proposed circuit is a new low-voltage and low-stress CMOS clock voltage doubler. Through the use of a dummy switch, the charge injection induced by the bootstrapped switch is greatly reduced resulting in improved sample-and-hold accuracy. An important attribute of the design is that the ON-resistance is nearly constant. A test chip has been designed and fabricated using TSMC 0.18 μm CMOS process (single poly, n-well) to confirm the operation of the circuit for a supply voltage down to 0.65 V.

**Key Words:** Reliable Low-Voltage CMOS Analog Design, deep submicron, clock booster, CMOS analog switches, bootstrapped CMOS switches.

## I. INTRODUCTION

Most analog-to-digital converters (ADC) typically employ a sample-and-hold circuit at the front-end that must achieve high speed, high linearity and high precision with low-power dissipation. In low-voltage systems, analog sampling becomes particularly difficult because the limited headroom severely degrades the tradeoffs among dynamic range, linearity, speed and power dissipation.

Among the most serious factors affecting the performance of a high precision CMOS sample-and-hold circuit are charge injection and clock feedthrough [1]-[2]. Several methods have been proposed to overcome these imperfections. These include charge cancellation by a dummy MOS transistor [3], offset cancellation by adding a compensation network, use of a closed-loop architecture, use of a Miller hold capacitance and finally use of switched-op-amp based sample-and-hold circuit [4]. Although charge cancellation methods that make use of a dummy transistor produce good simulation results, great care must be exercised when laying out the clock tree controlling the complementary switches. Other methods have either limited input bandwidth or introduce high design complexity.

Although the above techniques are useful and commercially available, it should be noted that they represent a tradeoff with respect to speed, power consumption and design flexibility. Alternatively, bootstrapped analog switches have been extensively used for rail-to-rail switching functions in low-voltage switched-capacitor (SC) circuits [5]. They show a constant charge injection through the whole range of operating supply voltage at

the expense of an input dependent clock feedthrough. This technique, however, introduces reliability problems, in particular, for devices with reduced oxide thickness ($t_{ox}$). Figure 4.2 shows the forecasted gate-oxide thickness as a function of time according to the Semiconductor Industry Association (SIA) roadmap [6].

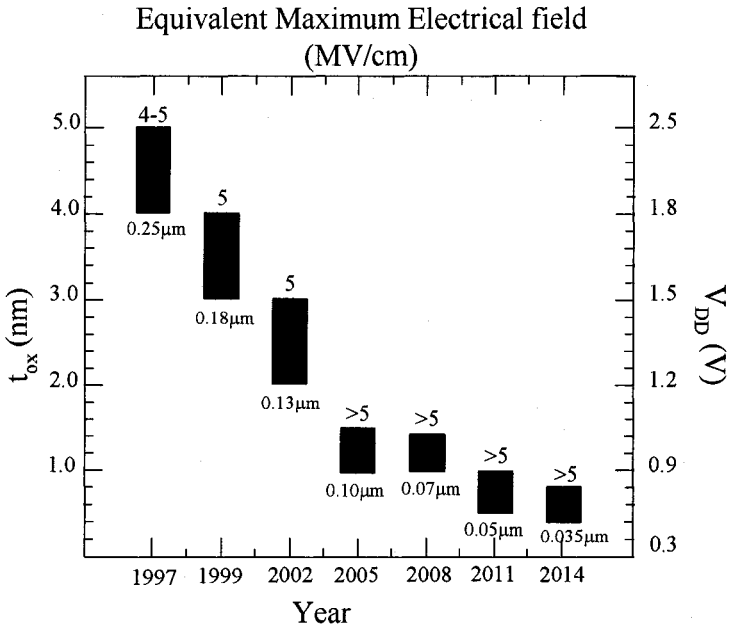



**Figure 4.2:** SIA forecast of MOS Gate oxide as a function of time.

It also displays the maximum electrical field across the oxide. The electrical field becomes increasingly high as $t_{ox}$ shrinks below 2 nm. It is important to note that oxide breakdown is one of the limiting factors for circuit reliability. Therefore utilization of the bootstrapped low-voltage analog switch for advanced VLSI processes will be limited in the next few years by the need for a low-stress clock voltage doubler circuit. To overcome these limitations we propose a novel low-voltage low stress and reliable clock

signal doubler. This clock doubler has been used in the implementation of a dummy compensated bootstrapped switch.

The reminder of this manuscript is a brief review of the basic principle of the analog low-voltage bootstrapped switch in Section 2, followed by the design consideration and physical layout guideline. Section 3 focuses on the results and section 4 on the conclusion.

## II. DEEP SUBMICRON LOW-VOLTAGE CMOS ANALOG SWITCH

A main characteristic of the MOS transistor is that it is an analog switch by itself. Transistors are extensively used as switches in switched capacitor circuit gain stages, capacitors and resistors D/A and so on. Drain and source terminals are the two switch terminals and the gate (and sometimes the bulk) terminals are used to control the conductivity. Ideally the switch in the on state acts as a fixed linear conductance $g_{ds}$. In practice, the conductance is strongly signal-dependent. Equation (4.1) gives the conductivity of the transistors in function of the power supply voltage $V_{DD}$ and the input signal.

$$g_{ds} = \begin{cases} kp_n \cdot \dfrac{W}{L} \cdot \left[ V_{DD} - V_{in} - V_{th,n} - \gamma_n \left( \sqrt{2\phi_f + V_{in}} - \sqrt{2\phi_f} \right) \right] & \text{nMOS} \\ kp_p \cdot \dfrac{W}{L} \cdot \left[ V_{in} - \left| V_{th,p} \right| - \gamma_p \left( \sqrt{2\phi_f + V_{DD} - V_{in}} - \sqrt{2\phi_f} \right) \right] & \text{pMOS} \end{cases} \tag{4.1}$$

The bulk of the nMOS and pMOS transistors are respectively connected to $V_{SS}$ and $V_{DD}$ unless otherwise stated. Plots in Figure 4.3 are the switch conductance versus input signal $V_{in}$. Figure 4.3a assumes that $V_{DD}$ is much larger than the sum of the two

threshold voltages $V_{th,n}$ and $V_{th,p}$. In this case, it is easiest to achieve a large conductance from rail-to-rail $V_{in}$. When $V_{DD}$ is comparable to the sum of the threshold voltages, there is a substantial drop in the conductance when $V_{in}$ approaches $V_{DD}/2$. Obviously, when the power supply is smaller than a critical value $V_{DD,\,crit}$, a gap appears at mid-range (Figure 4.3b), in which neither switch conducts. This critical value is given by:

$$V_{DD,\,crit} = |V_{th,p}| + V_{th,n} \tag{4.2}$$

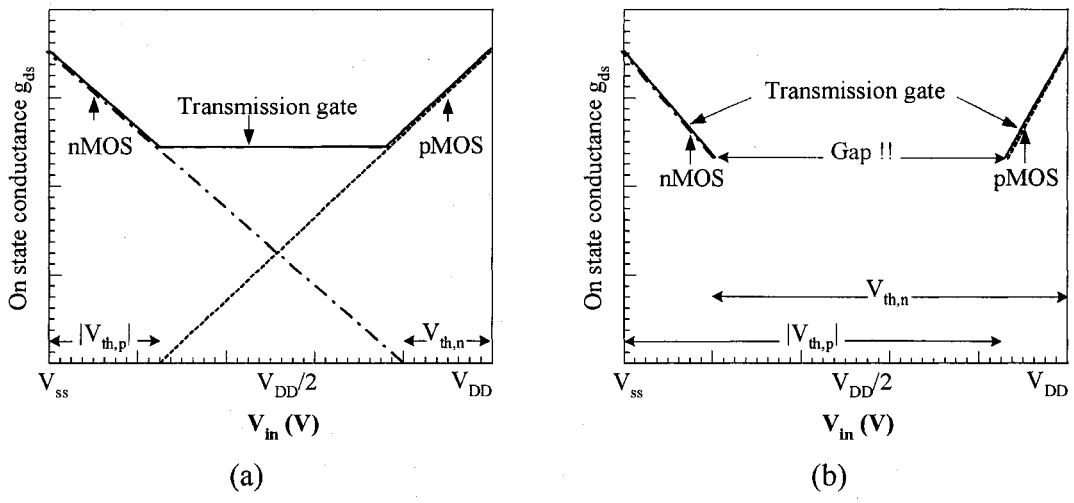



**Figure 4.3:** On state conductance of MOSFET switch versus the potential of the input signal: (a) low supply voltage, (b) for extremely low supply voltage.

As shown in Equation (4.1) and corresponding Figure 4.3, the switch conductivity depends not on the absolute potential of the control terminals, but on their potential relative to the others. Also the conductance through the whole range of input is not constant, and depends on the supply voltage, which becomes extremely low. To ensure rail-to-rail switching, control signals exceeding the supply voltage range are required.

This is known as the bootstrapped switching technique. An extended survey CMOS analog circuit suitable for low-voltage application and the bootstrapped switch is provided in [7]-[8].

### *A. Circuits description*

A general block diagram of the bootstrapped switch is shown in Figure 4.4. It consists of three main elements: the pass-transistor (nMOS, pMOS or both types), a control signal generator and, finally a clock booster. The control circuit generates a signal linearly related to the input signal. The purpose of the clock booster is to generate a clock signal over and above the supply voltage. In the classical case of a transmission gate, the clock booster and the control circuit are omitted.

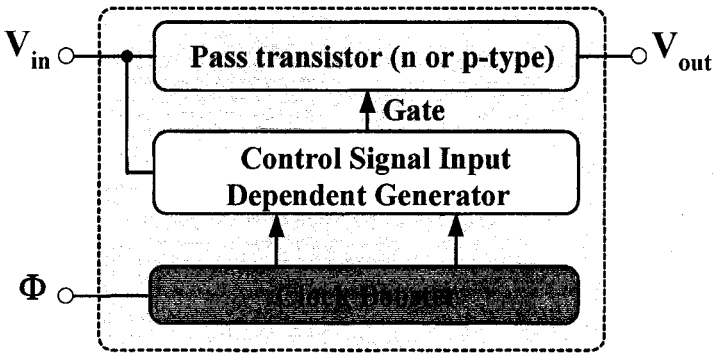



**Figure 4.4:** Block diagram of the bootstrapped switch.

Figure 4.5a illustrates the basic operation principle of a switched-capacitor clock signal booster. The switches are closed in pairs, alternatively. First the switches labelled $\phi_1$ are closed, charging capacitor $C_S$ to the input supply voltage $V_{DD}$ and discharging the

load capacitor $C_L$. Then the $\phi_1$ switches are opened and the $\phi_2$ switches are closed. This places $C_S$, which is previously charged to $V_{DD}$, in series with the supply voltage, producing a voltage $2V_{DD}$ across the output. The cycle then repeats. Applying the charge conservation principle, the output voltage $V(\phi_{bt2})$ on the load capacitor $C_L$ during $\phi_2$ is given by:

$$V(\phi_{bt2}) = 2V_{DD} \cdot \frac{C_S}{C_S + C_L} \tag{4.3}$$

$C_L$ includes the parasitic capacitances on the nodes driven by $\phi_{bt2}$. By minimizing those parasitics and choosing $C_S$ very large ($C_S \approx 8\ C_L$) an almost $2V_{DD}$ output voltage can be obtained. Note that the same topology can be used as a step-down clock signal converter, producing an output voltage less than the supply, by exchanging the input and output terminals.

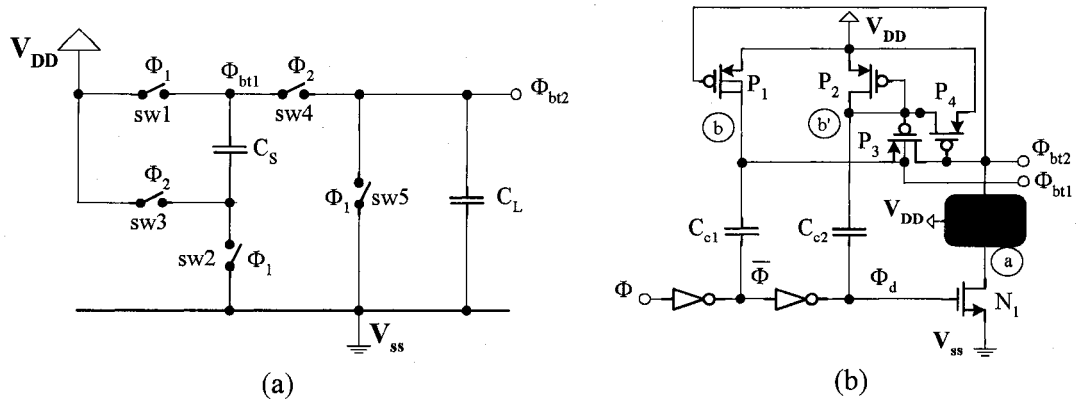
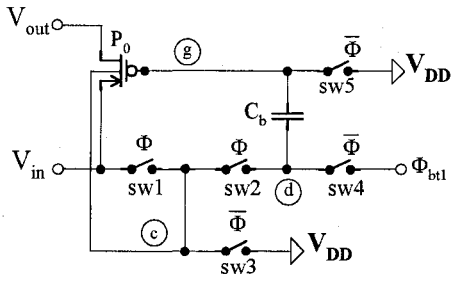
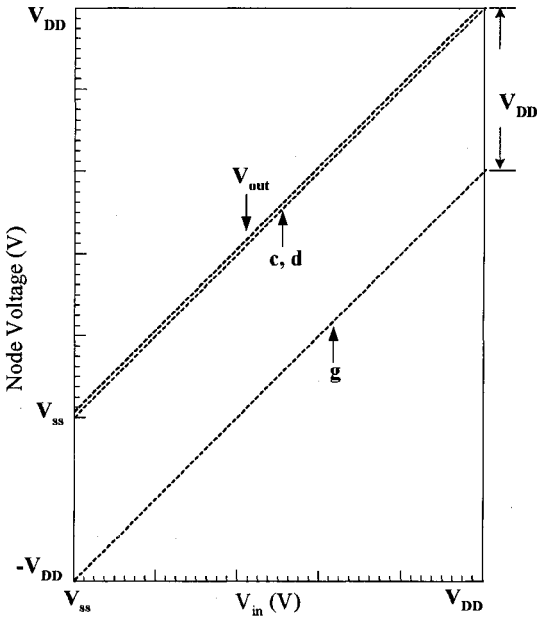



**Figure 4.5:** Clock voltage booster: (a) principle of operation, (b) CMOS circuit implementation.

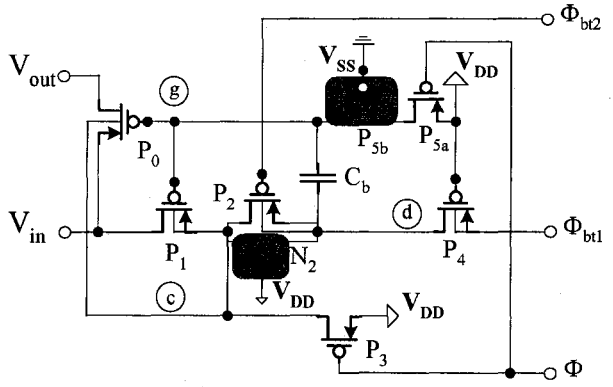
A CMOS implementation of clock booster is depicted in Figure 4.5b. When the input clock signal $\phi$ is high, the output signal $\phi_{bt2}$ is low while node b and b' are precharged to $V_{DD}$. When clock signal $\phi$ becomes low, node b is boosted to $2V_{DD}$, while node b' is discharged to $V_{DD}$-$|V_{th,p}|$ and the output signal becomes $2V_{DD}$. Feedback transistor $P_4$ keeps the gate-drain voltage of transistor $P_3$ to a reasonably low level and is subjected to a maximum source-gate voltage of $V_{DD}+|V_{th,p}|$, which is acceptable in most processes. The purpose of transistor $N_2$ is to keep the gate-drain voltage of $N_1$ far below $2V_{DD}$ in the off state; thus preventing its breakdown. However, $N_2$ is subject to a slightly high drain-source voltage $V_{DD}+ V_{th,n}$. Special care is needed in the layout and sizing of this device.




(a)




(b)




(c)

**Figure 4.6:** Bootstrapped switch: (a) principle of operation, (b) interval voltage variation, (c) pMOS-type pass transistor implementation.

The bootstrapped switch necessitates the generation of a control signal linearly dependent to the input signal in order to ensure a relatively constant conductance. To obtain constant-conductance operation, the gate-to-channel voltage should preferably be held constant during the on state. This can be accomplished using the bootstrap technique of Figure 4.6a [5]. In the off state ($\phi$-low), the bootstrap capacitor $C_b$ is charged to the supply-voltage difference ($2V_{DD}$-$V_{DD}$) through switches sw4 and sw5, and acts as a floating battery in the on state. The pass transistor, $P_0$, does not conduct because sw5 (respectively sw3) connects the gate and bulk terminals to the high supply potential $V_{DD}$. In the on state, the switches sw1 and sw2 connect the fully-charged bootstrap capacitor $C_b$ between $P_0$'s gate and source terminals. The bulk terminal of $P_0$ is also connected to the input driven voltage canceling the body-effect in first approximation. Applying again the charge conservation principle, $P_0$'s gate driven signal g is given by:

$$V(g) = V_{IN} - V_{DD} \tag{4.4}$$

Note, the difficulty lies in the implementation of the internal switches, particularly (not exclusively) sw1 and sw2 which must also be able to conduct in the rail-to-rail range. Figure 4.6b depicts the voltage variation at internal nodes c, d and g for input voltage varying from $V_{SS}$ to $V_{DD}$. The circuit level implementation is shown in Figure 4.6c. Transistor $P_{5b}$ prevents the gate breakdown of $P_{5a}$ and reduces its drain-source voltage in the off state. Regarding the difference between the pMOS-type or nMOS-type pass transistors, several issues have to be considered and the most important from the dynamic linearity viewpoint can be summarized as being the on-resistance $R_{ON}$, the channel charge $Q_{CH}$ and the junction capacitance $C_J$. All of these parameters scale with the switch size in the n-well process used ($kp_n \approx 4 \times kp_p$, $kp = \mu C_{ox}$). nMOS device allows to optimize the switch size as compared to pMOS. For the same dimensions, the nMOS presents lower $R_{ON}$ compared to pMOS while exhibiting similar $Q_{CH}$ and $C_J$ to first order. Parameters $g_{ds}$ (ON-state conductance) and $Q_{CH}$ give more precise data. In fact, conductance of pMOS transistor $P_0$ (Figure 4.6b) is given by Equation (4.5)

$$g_{ds} = kp_p \cdot \frac{W}{L} \cdot \left(V_{DD} - \left|V_{th,p}\right|\right) \tag{4.5}$$

It can also be derived in first order approximation that the channel charge $Q_{CH}$ is given by:

$$Q_{CH} = \begin{cases} -WLC_{OX} \cdot \left[ V_{DD} - V_{th,n} - \dfrac{\gamma_n}{2 \times \sqrt{2\phi_f}} V_{in} \right] & \text{nMOS} \\ -WLC_{OX} \cdot \left[ V_{DD} - \left| V_{th,p} \right| \right] & \text{pMOS} \end{cases} \tag{4.6}$$

Compared to its counterpart nMOS implementation, the pMOS exhibits a relatively constant conductance and channel charge independent of the input signal. In addition, it can be easily compensated. Hence, a pMOS is used as the pass device and Equation (4.5) shows that this circuit can operate at supply voltage close to $|V_{th,p}|$.

Before introducing the block diagram of the compensated bootstrapped switch circuit, let us examine the channel charge and clock feedthrough errors voltage in bootstrapped low-voltage analog switches and show that the dummy compensation can satisfy the proposed design. The mechanism for charge injection and clock feedthrough can be illustrated with the help of Figure 4.7a. When a MOS bootstrapped switch is ON, it operates in a triode region and has approximately zero voltage drop across the drain and source. There is a finite and nearly signal independent amount of channel charge $Q_{CH}$ in the inversion layer underneath the gate given by Equation (4.6). A fraction $\alpha$ of the channel charge will flow into $C_h$ and a voltage change $\Delta V_1$ is induced in the output node given by Equation (4.7):

$$\Delta V_1 = \frac{\alpha \times Q_{CH}}{C_h} \tag{4.7}$$

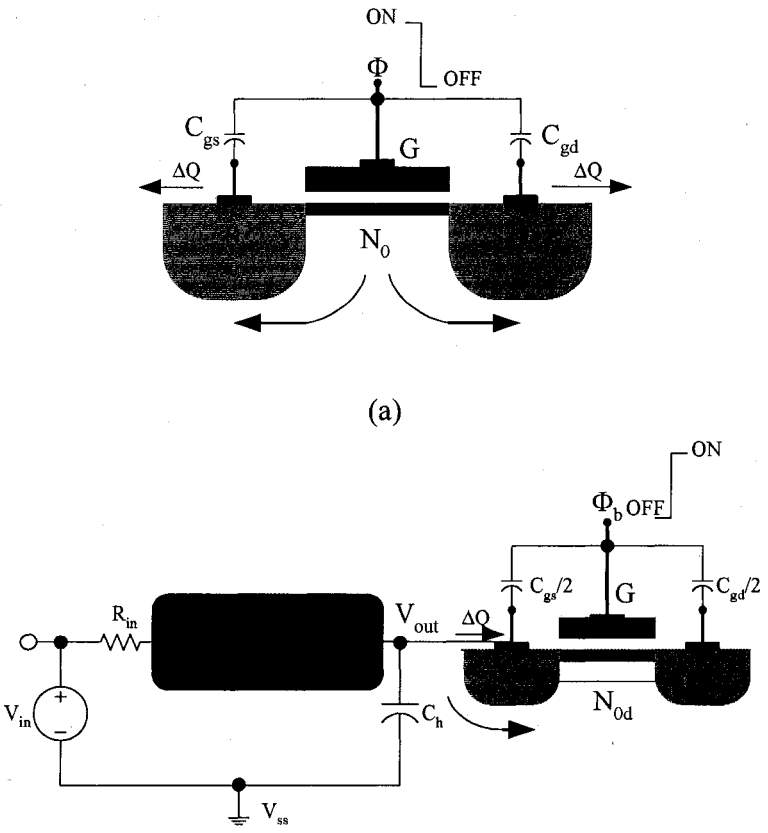



**Figure 4.7:** (a) Charge injection and clock feedthrough mechanism, (b) Charge error cancellation mechanism.

Similarly the clock feedthrough error $\Delta V_2$ due to the overlap and fringe capacitance is given by Equation (4.8), where $C_p$ stands for the parasitic capacitance ($C_{gd}$, $C_{gs}$ and others) and $V_{in}$ is the input signal:

$$\Delta V_2 = \begin{cases} -\dfrac{C_p}{C_h + C_p} \cdot (V_{in} + V_{DD}) & \text{nMOS} \\ -\dfrac{C_p}{C_h + C_p} \cdot (2 \times V_{DD} - V_{in}) & \text{pMOS} \end{cases} \tag{4.8}$$

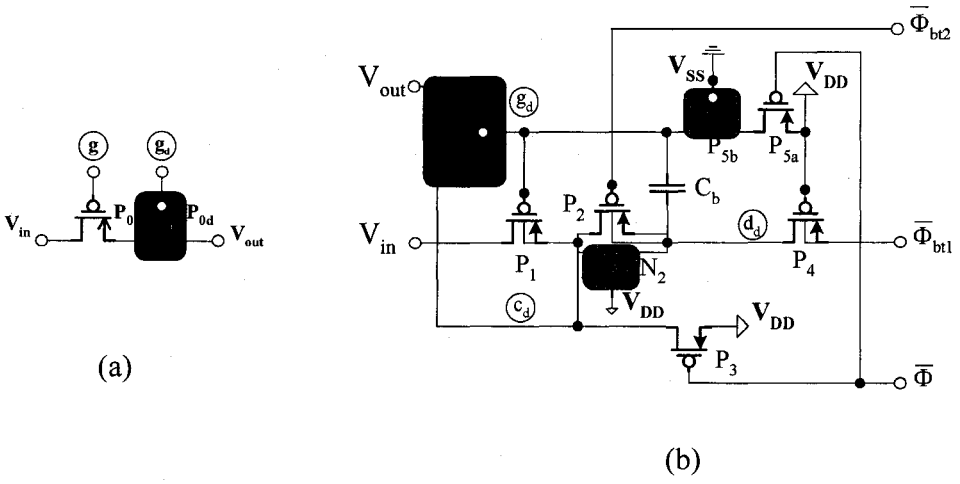



**Figure 4.8:** (a) Bootstrapped switch compensation scheme, (b) Dummy bootstrapped switch together with its control circuitry.

Contrary to channel charge injection error, clock feedthrough is largely input signal dependent. Clock feedthrough errors due to nMOS- type bootstrapped device increase with the input while decreasing with its counterpart pMOS- type device. Thus the overall voltage output change ΔV is slightly signal dependent. If, on the other hand, we are able to add a switch similar to the conducting one to the output node, the output voltage change can be greatly reduced. The charge injection contribution is removed. The mechanism is shown in Figure 4.7b where the dummy transistor $N_{0d}$ is added to absorb the charge coming from the main pass transistor $N_0$. The bootstrapped switch

compensation scheme is depicted in Figure 4.8a. The circuit consists of a pass-transistor $P_0$ with a dummy transistor denoted as $P_{0d}$ at the output node. Shown in Figure 4.8b is the dummy transistor $P_{0d}$ with its control signal circuitry. Design considerations and layout guidelines will be addressed in the following section.

### *B. Design Considerations and Physical layout guidelines*

Although it is difficult to derive an analytical set of design equations for the proposed circuit, some general design guidelines are given.

The capacitor value should be chosen as small as possible for area considerations but large enough to sufficiently charge the load to the desired voltage levels. As process technologies continue to scale down, lateral fringing becomes more important. The lateral spacing of the metal layers shrinks with scaling, while the thickness of the metal layers and the vertical spacing of the metal layers stay relatively constant. This means that structures utilizing lateral flux enjoy a significant improvement with process scaling, unlike conventional structures that depend on vertical flux [7]. A higher capacitance density can be achieved by using lateral flux capacitor as well as vertical flux. It is called fringing effects based capacitors and has been used to implement the capacitors in the design.

The devices sizes should be chosen to create sufficiently fast rise and falling times at the load. The load consists of the gate capacitance of the switching device $P_0$ (Figure 4.6a) and any parasitic capacitance due to the interconnect between the bootstrap circuit and this device. Therefore, it is desirable to minimize the distance between the bootstrap

circuit and the switch in the layout. Once the load is known, other device sizes can be chosen. Capacitors $C_{c1}$ (Figure 4.5c) must be sufficiently large to supply charge to the gate of the switching device in addition to all parasitic capacitances in the charging path including $C_b$ (Figure 4.6b).

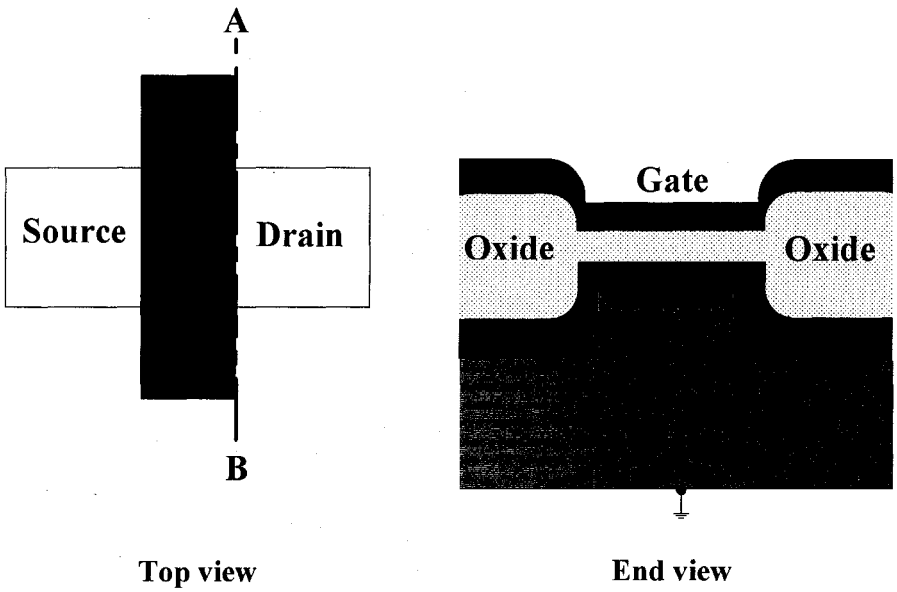



**Figure 4.9:** Weakest region of drain reverse breakdown.

The reliability of the circuit (clock booster-bootstrap circuit) can be further improved by carefully laying out some of the critical devices. Although the relative voltages between gate, source, and drain do not exceed $V_{DD}$, the drain-to-substrate and source-to-substrate voltages of some devices exceed $V_{DD}$ (assuming n-well process). Devices $N_{b2}$ (Figure 4.5b) and $N_2$ with $P_{5b}$ (Figure 4.6c) are subjects to this large voltage. Typically a CMOS technology is designed such that the reverse breakdown of a stand-alone n+/p- junction is approximated $3V_{DD}$ [9]. This voltage called $BV_{SS}$ is tested

under the condition that the gate and source are grounded. In an nMOS, however, a n+/p+ junction is formed between the n+ drain (or source) and the p+ channel-stop implant.

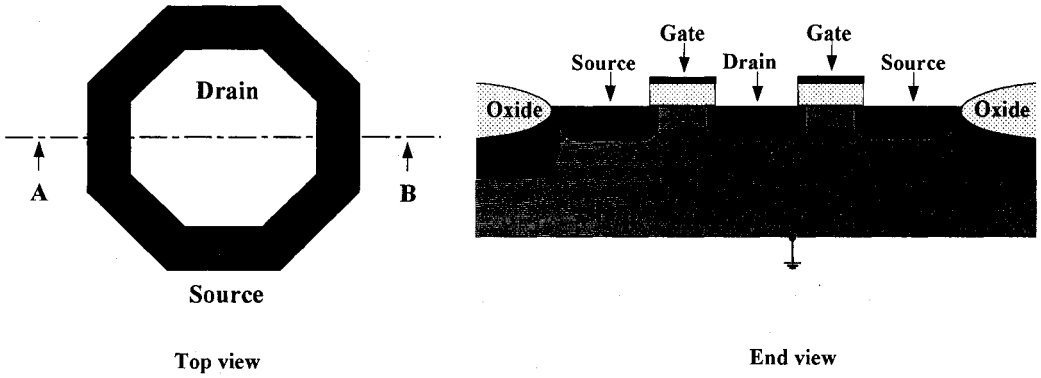



**Figure 4.10:** Circular or "doughnut" drain layout.

This breakdown voltage is further reduced when it is under a thin oxide as shown in Figure 4.9. The right-hand side of Figure 4.9 shows a cross-section of the transistor through plane AB. The breakdown in this region is typically designed to 1.7 $V_{DD}$ [9]. Using a circular drain or "doughnut" layout (Figure 4.10), the p+ channel stop can be removed around the drain to add another 1-2 V to the breakdown voltage [9]. Thus, for improved reliability, the drain of devices $N_{b2}$ (Figure 4.5b) and $N_2$ with $P_{5b}$ (Figure 4.6c) should be laid out circularly. The "doughnut" transistor structure also has the advantage of being area efficient with less parasitic capacitance at the drain making this structure attractive for high-speed applications [1], [9], [10]. Finally, the "off" drain-source voltage of $N_{b2}$ and $P_{5b}$ can exceed $V_{DD}$ introducing a potential punch-through problem.

If, however, the channel length of this device is increased (typical $1.5 \times L_{min}$) this punch-through voltage can be increased significantly beyond the nominal supply voltage.

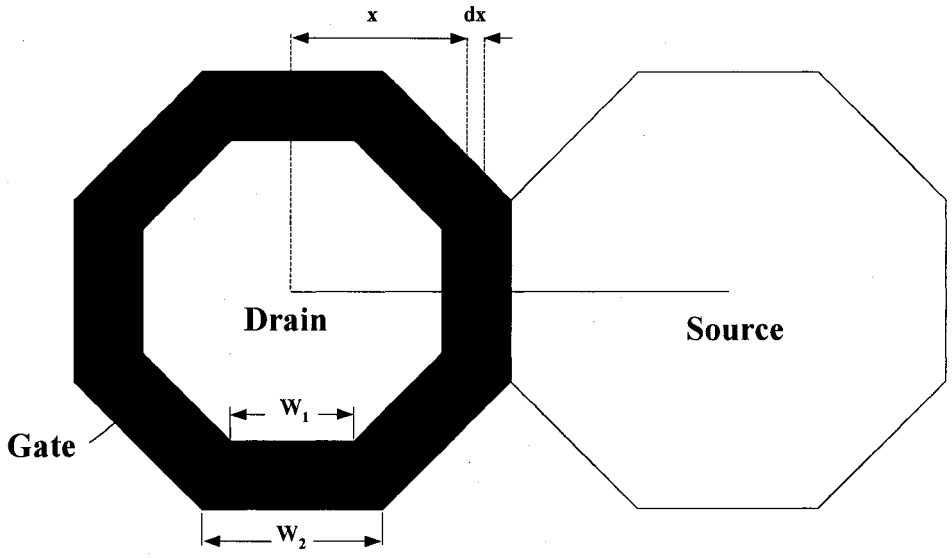



**Figure 4.11:** Calculation of the effective width for "doughnut" transistor.

Before the "doughnut" transistor can be effectively used in circuit design, the effective W/L ratio has to be determined. This ratio will be approximated by integrating the current-voltage relationship for an infinitesimal distance dx over the total gate length of the transistor (Figure 4.11). The calculation is performed when the transistor operates at the transition point between the linear and the saturation region. In this case, the voltage drop along the channel is linear and $V_{GS}$-$V_{th}$ equals $V_{DS}$. Let's x be the horizontal position of a small element C the channel, measured from the drain (D) end. If we assume that the electrical field along the channel is constant, then:

$$\frac{V_{CS}(x)}{\frac{W_2}{2\tan\left(\frac{\pi}{8}\right)} - x} = \frac{V_{DS}}{\frac{W_2 - W_1}{2\tan\left(\frac{\pi}{8}\right)}} \tag{4.9}$$

where $W_1$ and $W_2$ are parameters of the octagonal shape, $V_{CS}$ with $V_{DS}$, the drain-to-source and channel-to-source voltage respectively.

Derivation of Equation (4.9) gives the incremental voltage drop, $dV_{CS}$, along the channel (with respect to the source)

$$dV_{CS}(x) = \frac{V_{DS}}{\frac{W_1 - W_2}{2\tan\left(\frac{\pi}{8}\right)}} dx \tag{4.10}$$

The incremental resistance depends on the mobile channel charge

$$dR_{DS} = R_{DS}\frac{dx}{W} = \frac{1}{\mu Q_m(x)}\frac{dx}{W} \tag{4.11}$$

From Figure 4.11, the width W of the infinitesimal element dx is given by

$$W = 2x\tan\left(\frac{\pi}{8}\right) \tag{4.12}$$

The mobility charge $Q_m$ (x) for strong inversion is given by

$$Q_m(x) = C_{ox}\left[V_{GS} - V_{th} - V_{CS}(x)\right] \tag{4.13}$$

The current through the channel is proportional to the voltage drop $dV_{CS}$ (x) across the resistance $dR_{DS}$

$$I_{DS} = \frac{dV_{CS}(x)}{dR_{DS}(x)} \tag{4.14}$$

Using (4.10), (4.11), (4.12) and (4.13), Equation (4.14) becomes

$$I_{DS} = \mu C_{ox}\left(\frac{2\tan\frac{\pi}{8}}{W_1 - W_2}\right)^2 x\left[W_1 - 2x\tan\frac{\pi}{8}\right]V_{DS}^2 \tag{4.15}$$

By integrating the current-voltage of relation (4.15), we obtain

$$I_{DS}\int_{\frac{W_1}{2\tan\frac{\pi}{8}}}^{\frac{W_2}{2\tan\frac{\pi}{8}}}\frac{dx}{x} = \mu C_{ox}\left(\frac{2\tan\frac{\pi}{8}}{W_1 - W_2}\right)^2 V_{DS}^2\int_{\frac{W_1}{2\tan\frac{\pi}{8}}}^{\frac{W_2}{2\tan\frac{\pi}{8}}}\left[W_1 - 2x\tan\frac{\pi}{8}\right]dx \tag{4.16}$$

Taking into account the eight sides of the octagonal, the current-voltage characteristic is given by

$$I_{DS,\text{total}} = 8I_{DS} = 8\frac{\left(2\tan\left(\frac{\pi}{8}\right)\right)}{\ln\left(\frac{W_2}{W_1}\right)}\frac{\mu C_{ox}}{2}\left(V_{GS} - V_{th}\right)^2 \tag{4.17}$$

Therefore the effective W/L ratio is

$$\left[\frac{W}{L}\right]_{eff} = 8\frac{\left(2\tan\left(\frac{\pi}{8}\right)\right)}{\ln\left(\frac{W_2}{W_1}\right)} \tag{4.18}$$

This equation links the geometrical parameters $W_1$ and $W_2$ of the gate all-around transistor to its effective W/L ratio.

From Figure 4.11, it appears that the channel length L (which do not correct for corner effects) for an octagonal shape with parameter $W_1$ and $W_2$ is given by:

$$L = \frac{W_2 - W_1}{2\tan\frac{\pi}{8}} \tag{4.19}$$

Inversely for a given effective W/L ratio, the geometrical parameters $W_1$ and $W_2$ can be computed using

$$W_1 = \frac{2\tan\frac{\pi}{8}}{K-1}L \tag{4.20}$$

$$W_2 = K\frac{2\tan\frac{\pi}{8}}{K-1}L \tag{4.21}$$

where

$$K = \exp\left\{8\left(2\tan\frac{\pi}{8}\right)\left[\frac{L}{W}\right]_{eff}\right\} \tag{4.22}$$

Equations (4.20) and (4.21) are used in the laying out process of the "doughnut" or octagonal shape transistor. A similar equation has been derived by Anne Bosch [10] for a hexagonal transistor. In [11], an analytical expression for the W/L ratio can be found for transistors with nonrectangular gate geometry. However, the analysis is more complex.

## III. Simulation and Experimental Results

The implementations of described modules (switches and clock booster) have been simulated with Hspice using BSIMv3 for two different technologies. In 0.5μm AMI Semiconductor Inc technology the mean value threshold voltages are approximately 0.86 V and –1 V for nMOS and pMOS transistors, respectively, whereas in the 0.18 μm technology they are approximately 0.52 V and –0.48 V, respectively. In the 0.18 μm

CMOS process, metal-metal capacitors are used in the implementation of capacitors $C_{c1}$, $C_{c2}$ and $C_b$ because of the non-availability of poly-poly capacitors.

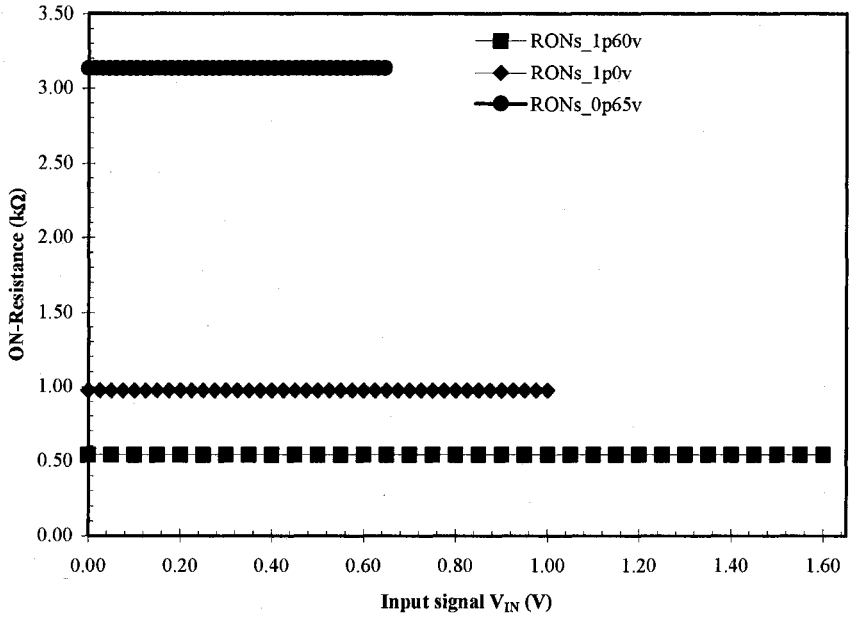



**Figure 4.12:** Simulated switch ON-resistance variation with supply voltage (0.18 μm CMOS digital process).

Figure 4.12 shows a ON-resistance variation with supply voltage in the 0.18μm process. RON_1p60 denotes the ON-Resistance of the switch when simulated with a supply voltage $V_{DD}$ = 1.60 V. For ultra low-voltage ($V_{DD}$ < 0.7 V), the transmission gate formed by $P_2$ and $N_2$ (Figure 4.6c), induced a dead band region which introduces a small variation on the conductance (Figure 4.13). Figure 4.14 presents the simulated dependence of the feedthrough error voltage with respect to the analog input under 1 V

operation condition and 1 MHz sampling clock frequency. An almost linear variation is observed. This result is in concordance with relation (4.8).

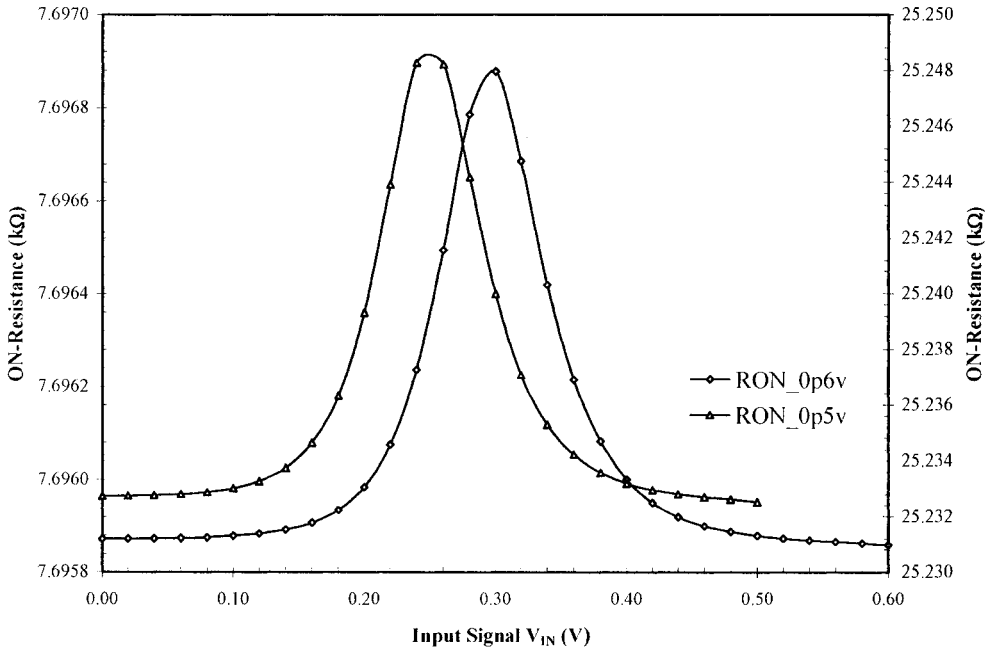



**Figure 4.13:** Simulated switch ON-resistance variation for ultra-low supply voltage ($V_{DD} < 0.7V$).

The dummy compensation mechanism removes the charge injection contribution from the observed voltage error. Even if this charge injection is not completely removed, it has been demonstrated that it is signal-independent (Equation 4.6) and thus appears as a constant offset at the output. A fully differential-based implementation will remove the residual offset voltage. To further evaluate the non-linearity, we generated the power spectral density (PSD) of the sample-and-hold output signal via Matlab. A total of N =

256 ($2^8$) data samples were used with 35 signal cycles to ensure the coherency sampling requirement [12].

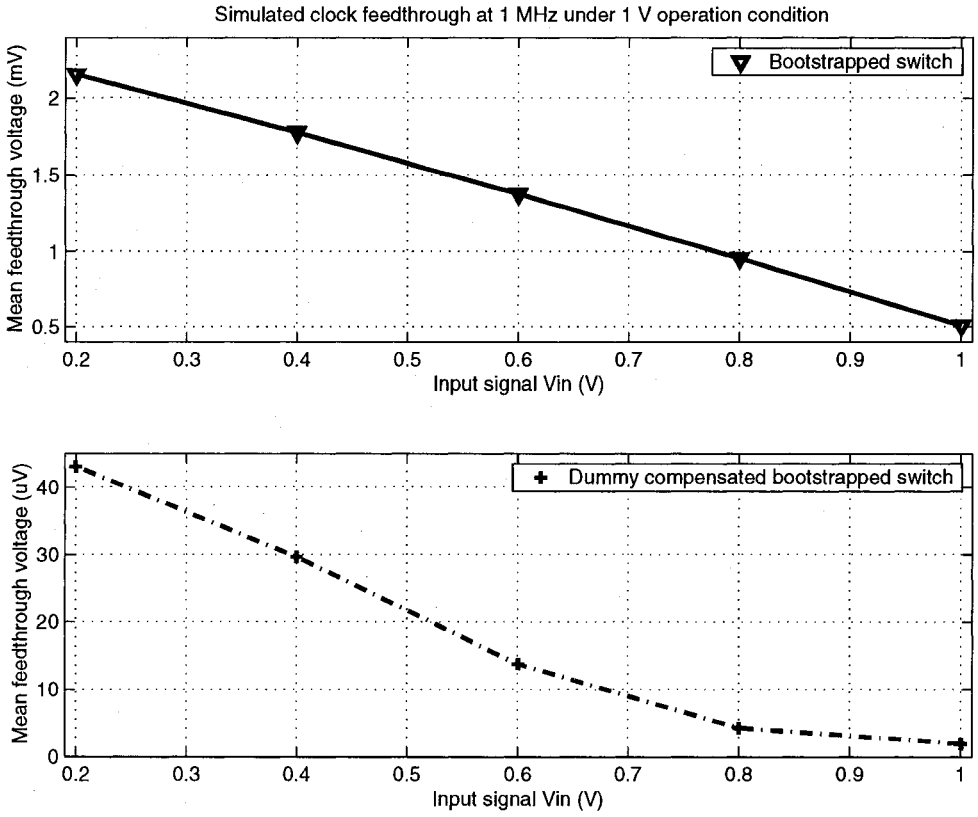



**Figure 4.14:** Simulated dependence of the feedthrough voltage on the analog input.

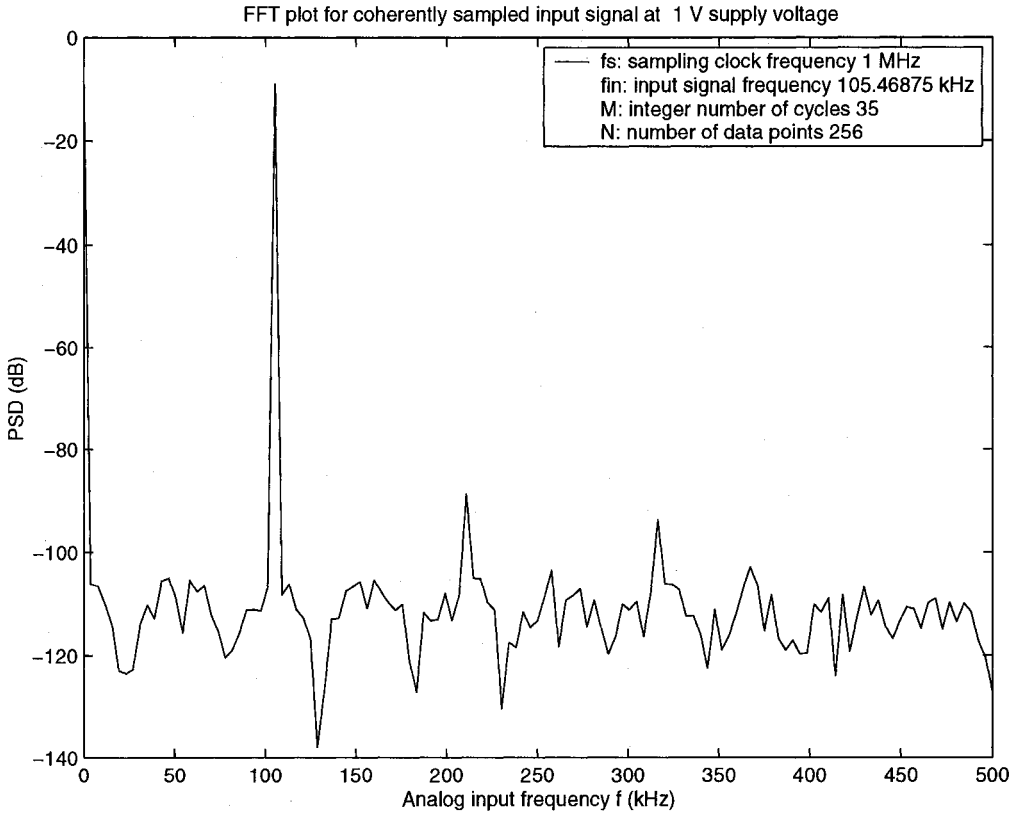



**Figure 4.15:** Simulated spectrum of the compensated bootstrapped switch under a sampling frequency of 1 MHz, an input frequency of 105.46875 kHz and a signal amplitude of 1 $V_{PP}$ under a supply voltage $V_{DD}$ = 1 V.

Figure 4.15 shows the simulated spectrum of the compensated bootstrapped switch under a sampling frequency of 1 MHz and 1 V supply voltage using a load capacitance of 5 pF. The corresponding SNDR and THD are respectively 77.8178 dB and –78.40 dB. The simulated transfer function of the compensated switch is displayed in Figure 4.16. A test chip was designed and fabricated with TSMC 0.18 μm CMOS process

(single poly, n-well) to confirm the operation of circuit topology and Figure 4.17 shows the die photography of the clock booster with the bootstrapped switch.

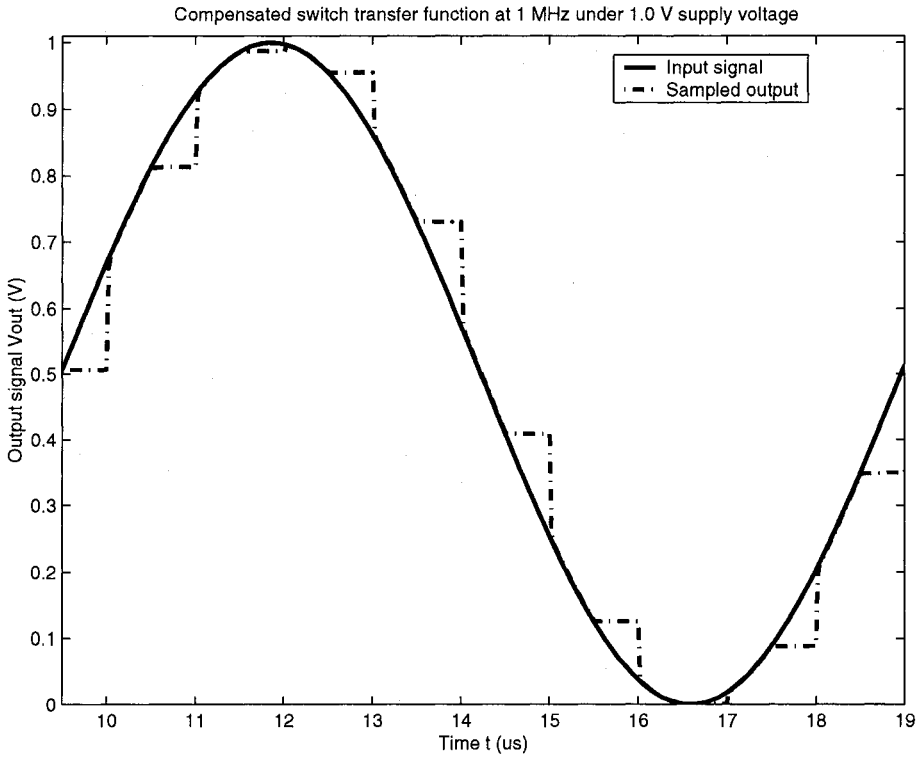



**Figure 4.16:** Simulated input/output of the bootstrapped switch under a sampling frequency of 1 MHz, an input frequency of 105.46 kHz and a signal amplitude of 1 $V_{PP}$ under $V_{DD}$ = 1 V.

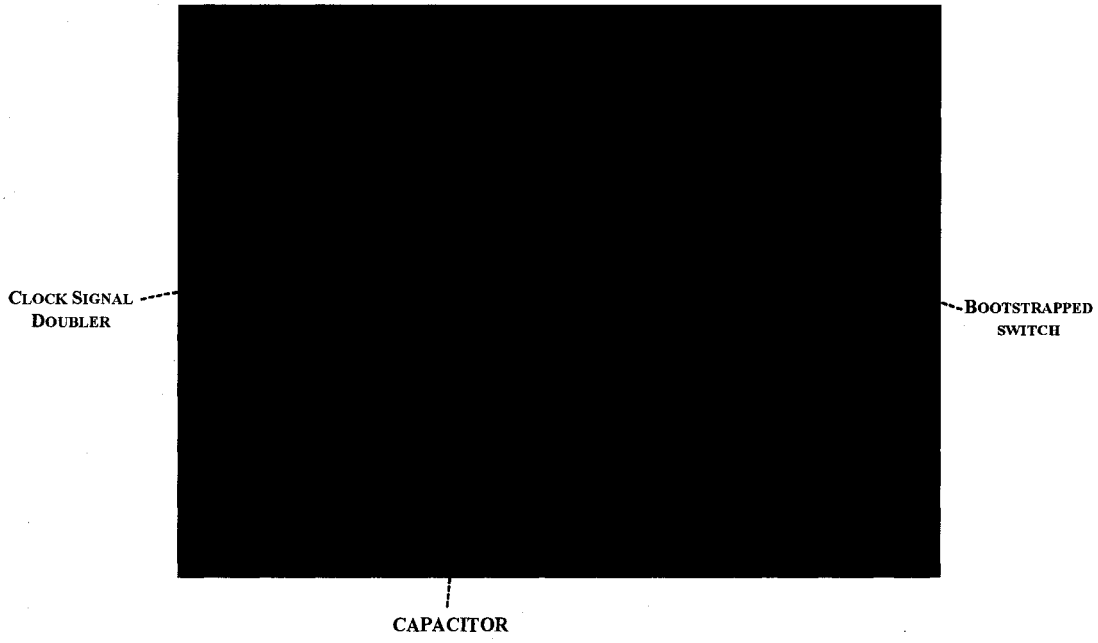



**Figure 4.17:** Photography of the test chip.

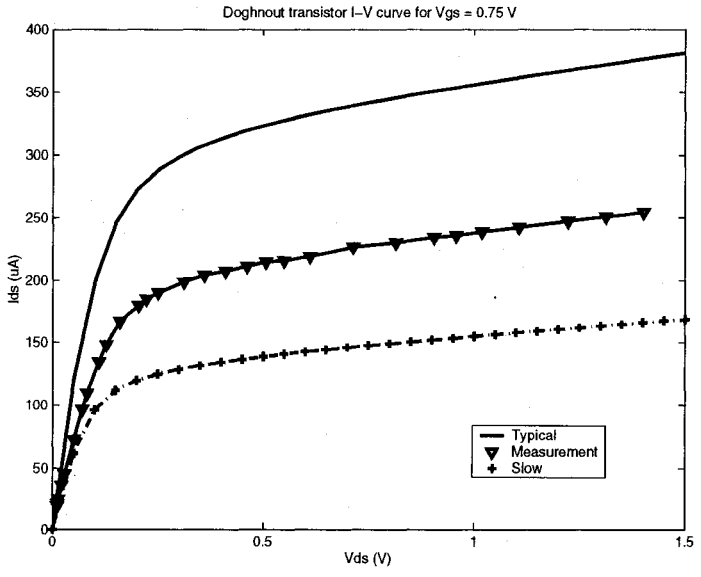



**Figure 4.18:** "Doughnut" transistor characteristics $I_{DS} = f(V_{DS})$ for $V_{GS} = 0.75$ V.

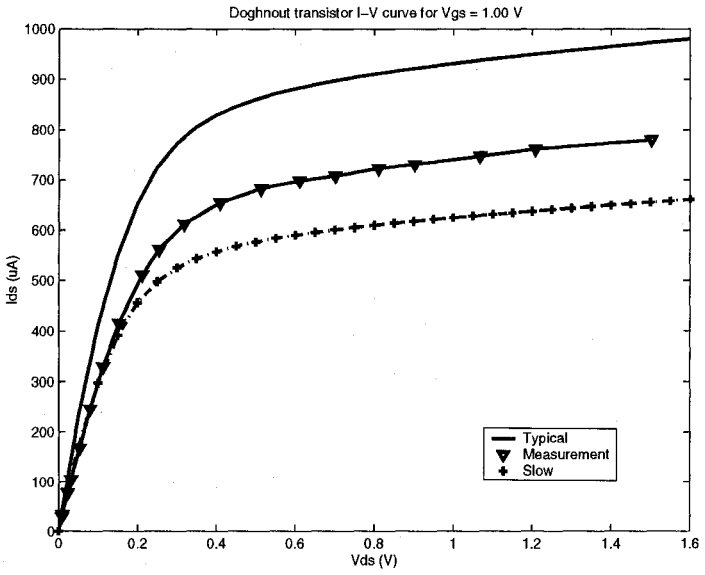



**Figure 4.19:** "Doughnut" transistor characteristics $I_{DS} = f(V_{DS})$ for $V_{GS} = 1.0$ V.

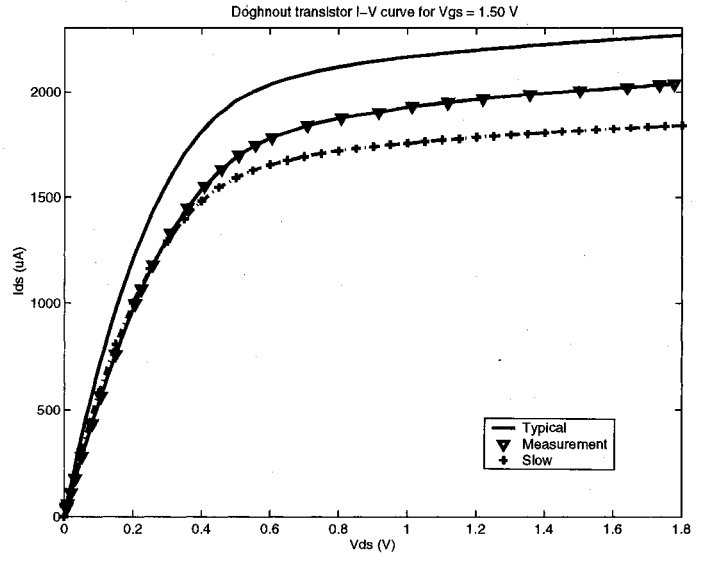



**Figure 4.20:** "Doughnut" transistor characteristics $I_{DS} = f(V_{DS})$ for $V_{GS} = 1.5$ V.

Measured $I_{DS} = f(V_{DS})$ characteristics of an octagonal "doughnut" transistor ($W_1$= 0.60 μm, $W_2$= 0.77 μm, L = 0.20 μm) compared with the simulation results of its equivalent rectangular transistor having an aspect ratio $[W/L]_{eq}$ of 4.30μm/0.2μm are shown in Figures 4.18, 4.19 and 4.20. The measurements were compared with a slow and typical device model. The deviation from the typical values is mainly due to the mismatch between the exact transistor size and the physical layout dimension.

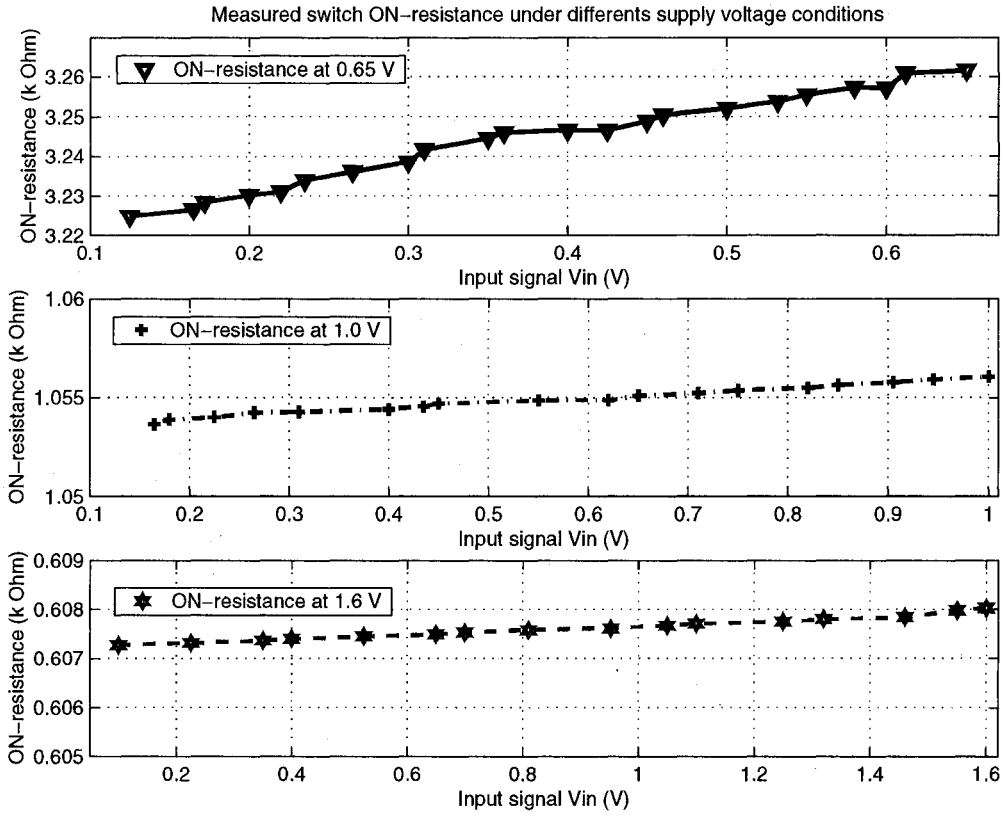



**Figure 4.21:** Measured ON-resistance under 0.65, 1.0 and 1.60 V supply voltages.

Figure 4.21 presents the measured switch ON-resistance under a 0.65, 1.0 and 1.60 V operating supply voltages. An almost constant ON-resistance is obtained. Under a

0.65 V operating condition, a typical variation of 0.38 Ω is observed for input signal varying from 0.125 V to 0.65 V.

**ch1**: Sine wave input signal **ch2**: Sampled output signal

**Figure 4.22:** Measured input-output waveform of the bootstrapped switch circuit test chip with a sampling speed of 0.5 MHz, an input frequency of 82.031 KHz and a signal amplitude of 1 V under a supply voltage $V_{DD}$ =1 V.

Measured waveform of Figure 4.22 shows the circuit performing sample-and-hold operation (sampling speed of 0.5 MHz, an input frequency of 82.03125 KHz) of an input signal amplitude of 1-V under a supply voltage of $V_{DD}$ = 1 V.

**ch1**: Sine wave input signal **ch2**: Sampled output signal

**Figure 4.23:** Measured input-output waveform of the bootstrapped switch circuit test chip with a sampling speed of 0.5 MHz, an input frequency of 82.031 KHz and a signal amplitude of 0.65 V under a supply voltage $V_{DD}$ =0.65 V.

Figure 4.23 depicts the characteristic for the same parameters except the input signal and the supply voltage $V_{DD}$ are at 0.65-V each. Under 0.25 MHz sampling condition, the measured SNDR obtained for a supply voltage of about 1.0 V and 0.65 V is 71.0527 dB and 45.775 dB, respectively. This corresponds to an effective resolution

of 11.5 bits and 7.3 bits, respectively. Operation of the circuit is possible at 10 MHz sampling frequency under a 1-V supply voltage; however special care is needed in the board design and test setup to clearly capture such waveform.

## IV. CONCLUSION

In this paper a design technique for low-voltage analog switch in deep submicron standard CMOS has been presented. The circuit is suitable for low-voltage and high-speed sample-and-hold circuit. The heart of this circuit is a new low-voltage and low-stress CMOS clock voltage doubler. An important attribute of the design is that the ON-resistance, is nearly constant. A test chip has been implemented and fabricated using TSMC 0.18 μm CMOS process (single poly, n-well) to confirm the operation of the circuit for a supply voltage down to 0.65 V. The rail-to-rail input range capability enables the circuit to be used in high-speed such as flash, successive approximation and pipelined ADCs, to name just a few examples.

**ACKNOWLEDGMENTS**

The authors would like to acknowledge the financial support from the Natural Sciences and Engineering Research Council of Canada (NSERC), the Canadian Microelectronic Corporation for fabricating the test chips and Micronet.

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In the present chapter, implementation and subsequent experimental validation of low-voltage analog CMOS switch based on gated bootstrapped method is described. The next chapter will focus on design strategy for the implementation of analog MOS comparators, digital-to-analog and analog-to-digital converters operating at low power supply voltage (1-V and below).

# *Chapter 5*

# *LOW-VOLTAGE TECHNIQUES AND OTHER ANALOG BUILDING BLOCKS IN DEEP SUBMICRON CMOS*

Constraints imposed by advanced IC process technologies, modern electronic system requirements, and the economics of circuit integration have created new challenges in analog circuit design. With the advancement of CMOS process technologies into the ultra deep submicron (UDSM) realm and the increasing popularity of battery-powered mobile electronic systems comes the demand for lower-voltage analog circuit designs. In addition, the drive to reduce costs is forcing the integration of both analog and digital circuitry onto a single die. Both of these changes have a detrimental impact on the analog circuit performance. New analog design techniques and methodologies have been devised to enable high performance analog signal processing in today's environment. The purpose of this chapter is to describe state-of-the-art techniques and methodologies used to design opamp and analog CMOS comparators as well as the implementation of a 10-bit successive approximation ADC in submicron process.

## 5.1 Low-voltage rail-to-rail input/output opamp design

A fundamental building block in low-voltage analog design is the operational amplifier. Unlike the transconductance operational amplifier, it includes an output stage capable of driving off-chip resistive loads. Obviously, the output stage must respect the specification requirement for drive capability, linearity and output swing. Another critical aspect in low-voltage design is the common-mode input swing, which depends on the input stage.

In order to maximize the dynamic range, a low-voltage amplifier must be able to deal with signal voltages that extend from rail-to-rail. Such efforts have been underway for several years now [HOG94]. In CMOS op amp circuits, improved input range operation has been achieved by connecting complementary (nMOS and pMOS) differential amplifiers in parallel. However at extremely low-voltage supply (1-V and below) classical solutions are being replaced by new configurations [DUG00]. A novel design strategy based on a switched-capacitor arrangement is described here for an extremely low-voltage opamp circuit [FAY01a]. The block diagram of the opamp is shown in Figure 5.1. It consists of an input level shifter, a differential input pair and a dynamically biased class AB output stage to ensure a rail-to-rail output.

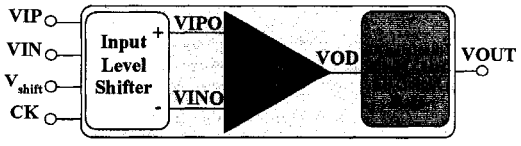



**Figure 5.1:** Low-voltage CMOS rail-to-rail input /output opamp block diagram.

### *5.1.1 Input level shifter circuit*

To overcome the limitation of the lower supply voltage constraint on deep sub-micron, the concept of dynamic level shifting has been proposed for bipolar operational amplifiers [FON89]. A similar method has been reported in [DUG00] for CMOS based operational amplifier circuits. These methods have been implemented in the continuous time domain and the level shifter circuit dissipates a static power. A switched-capacitor based approach is proposed here to realize the level shifting function and is depicted in Figure 5.2a with its clocking circuitry (Figure 5.2b). This limits the circuit to sample data applications.

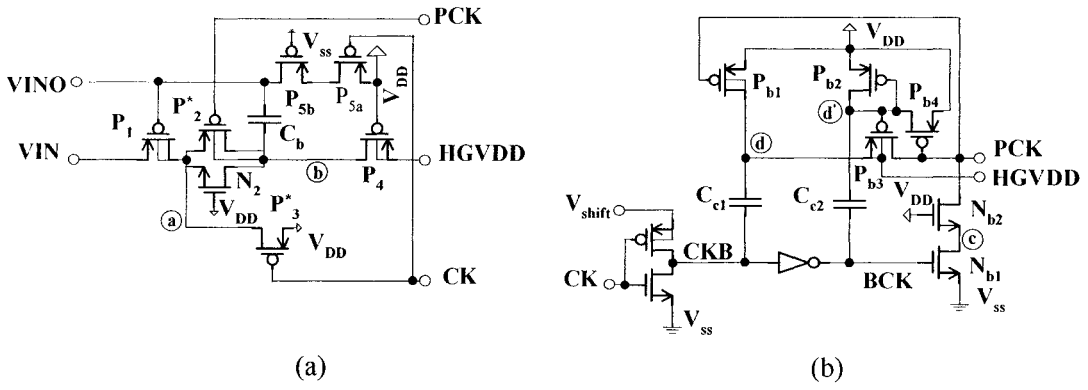



**Figure 5.2:** (a) pMOS input level shifter; (b) Clock booster circuit.

The level shifter circuit makes use of the control circuit of a pMOS bootstrapped constant impedance switch described in Section 4.2 (Chapter 4). When the clock signal is low, the gate voltage of the pMOS type input differential transistor is set to $V_{DD}$ and

therefore is off. At the same time node b is set to $V_{DD} + V_{shift}$. The charge $Q_{CH1}$ stored in capacitance $C_b$ is given by:

$$Q_{CH1} = C_b V_{shift} \tag{5.1}$$

where $V_{shift}$ , is an arbitrary voltage greater than the threshold of the pMOS input pair devices.

When the input clock signal goes high, the transmission gate formed by $N_2$ and $P^*_2$ starts conducting the input signal $V_{IN}$. Charge stored in capacitance $C_b$ thus becomes:

$$Q_{CH2} = C_b(V_{IN} - V_{INO}) \tag{5.2}$$

Using the charge conservation principle, the input drive voltage of the differential pair can be derived from (5.1) and (5.2) and is given by:

$$V_{INO} = V_{IN} - V_{shift} \tag{5.3}$$

Equation (5.3) shows that a linear relation exists between the input signal and the control voltage of the differential pair. The input voltage is therefore level-shifted down. The value of this voltage is low enough to turn on the differential pair at any input CM level and therefore suppresses the forbidden operation zone of the opamp (Figure 2.1c). $V_{shift}$ is an arbitrary value that is fixed so as to be able to drive the input differential pair. The linearity of the level-shifter circuit is ensured up to $V_{DD,\,crit}$ (see Equation 4.2), which is the limit imposed by the transmission gate formed by $P^*_2$ and $N_2$ (Figure 5.2a). This voltage is around 0.9-V in a standard 0.18μm CMOS process. The output range of the circuit is typically between -1 and 0 V for an input signal varying from 0 to 1 V and for

a $V_{shift}$ equal to 1 V. Reliability is not a concern since a 1.8 V technology is used at a 1 V supply voltage.

The functionality of the clock booster circuit is identical to the one used in the design of analog switches of section 4.2.

### *5.1.2. Differential input pair*

The input stage is shown in Figure 5.3. It is made up of the source- coupled pair M1-M2 and the folded cascode mirror (MN1-MN2). Transistors MS1 and MS2 have been added to enhance the slew-rate performance of the folded cascode circuit [JOH97].

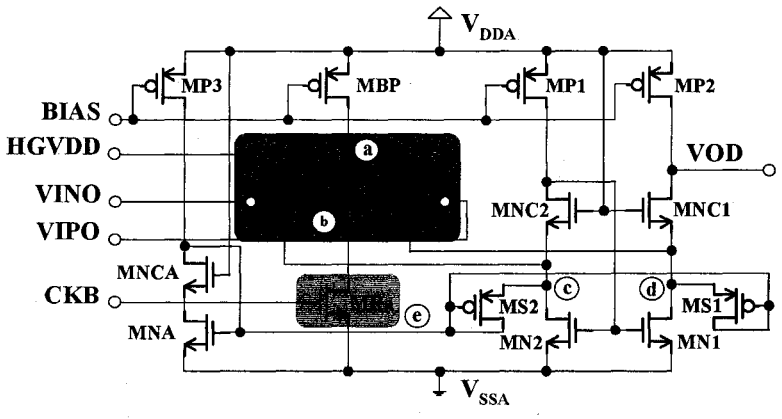



**Figure 5.3:** Low-voltage pMOS input stage.

When the operational amplifier is slew-rate limited, these transistors prevent the drain of M1 and M2 from having large transients that change their small-signal voltages to level very close to the positive power-supply voltage. The purpose of transistor MRa is to sink the biasing current of the input stage when the clock signal is low, thus avoiding this node being charged to $V_{DDA}$. However, this transistor can be removed without any dam-

age to the circuit. The body of the input source coupled transistors M1-M2 is tied to a high voltage $2V_{DDA}$. Assuming that the biasing current of the differential pair is $2 \cdot I_{BIAS}$, the source-gate voltage of transistor M1 (or M2) is given by:

$$V_{SG} - |V_{th,p}| = \sqrt{\frac{2I_{BIAS}}{\left(\mu C_{ox} \frac{W}{L}\right)_{M_1}}} \tag{5.4}$$

Remembering the fact that the gate-voltage of M1 is given by (4.26), the source-voltage of M1 (node a) is given by:

$$V_a = V_{IN} - V_{shift} + |V_{th,p}| + \sqrt{\frac{2I_{BIAS}}{\left(\mu C_{ox} \frac{W}{L}\right)_{M_1}}} \tag{5.5}$$

For a CM signal close to the negative supply voltage ($V_{SSA}$), and for a small value of bias current, the value of this voltage is close to that of node c. Therefore, the behavior of the circuit is no longer similar to that of a differential pair. Several solutions can be used. The first method is to increase the bias current level. This approach leads to an increase of the power dissipation of the circuit. The second solution is to use large length devices, which in turn increases the parasitic capacitance at this node and the overall circuit area. Another possibility is to slightly increase the threshold voltage of the source-coupled input pair device. This method has been adopted here since we have a voltage close to $2 \cdot V_{DDA}$ on-chip.

### *5.1.3 Class AB output stage*

A dynamically biased class AB output stage similar to the design reported in [GIU00] has been used and is shown in Figure 5.4.

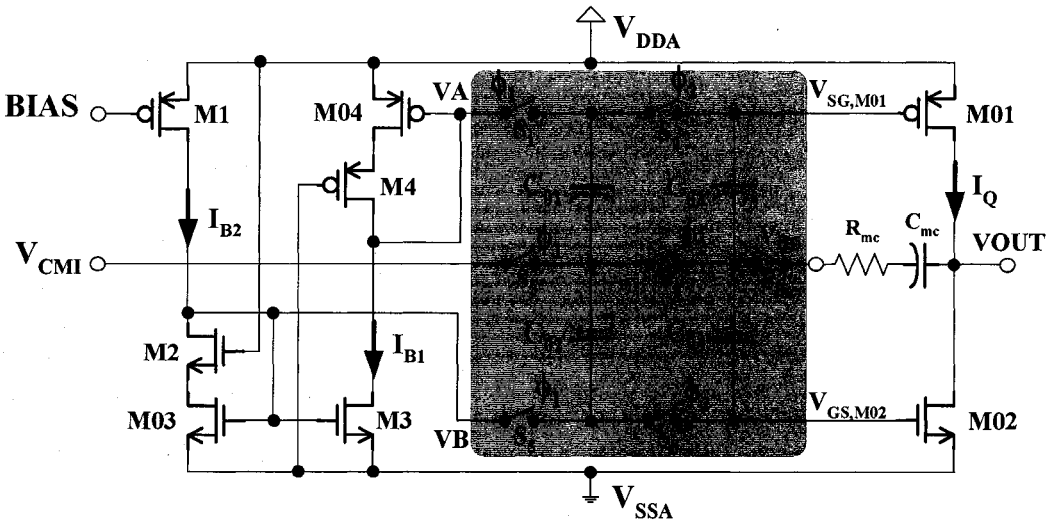



**Figure 5.4:** Low-voltage output stage.

Common source transistors M01 and M02 provide a rail-to-rail output swing, diode-connected transistors M03 and M04 set the bias voltages for the control of the quiescent current $I_Q$ in the output branch. The switched-capacitor (SC) network, composed of capacitors $C_{01}$-$C_{04}$ ($C_{01}$=$C_{02}$ and $C_{03}$=$C_{04}$) and switches $S_1$-$S_6$, performs a dynamic biasing [HOS80], [PAL00] and feeds by the input bias voltage $V_{OD}$ (differential pair output signal). Switches $S_1$-$S_6$ are controlled by complementary non-overlapping clock phase $\phi_1$ and $\phi_2$ and are implemented with nMOS transistors. Clock signals $\phi_1$ and P $\phi_2$ are boosted-signal generated by circuit similar to the one of Figure

5.2b. Switch $S_{mc}$ has been added to reduce the output capacitance seen by node VOD and thus increases the circuit unity gain bandwidth (UGBW).

Assuming standby conditions, capacitors $C_{01}$, $C_{03}$ with switches $S_1$-$S_4$ and capacitors $C_{02}$, $C_{04}$ with switches $S_3$-$S_6$ perform as two SC integrators.

During clock phase $\phi_1$, charge stored in capacitors $C_{01}$-$C_{04}$ are respectively given by:

$$\begin{cases} Q_{C_{01}}^{\phi_1} = C_{01}\left(V_A - V_{CMI}\right) \\ Q_{C_{02}}^{\phi_1} = C_{02}\left(V_B - V_{CMI}\right) \\ Q_{C_{03}}^{\phi_1} = C_{03}\left(V_{SG,M01}^{\phi_1} - V_{OD}\right) \\ Q_{C_{04}}^{\phi_1} = C_{04}\left(V_{GS,M02}^{\phi_1} - V_{OD}\right) \end{cases} \tag{5.6}$$

where $V_{CMI}$ denotes in the common-mode voltage of the differential input pair.

During $\phi_2$, charge stored in those capacitors become

$$\begin{cases} Q_{C_{01}}^{\phi_2} = C_{01}\left(V_{SG,M01}^{\phi_2} - V_{OD}\right) \\ Q_{C_{02}}^{\phi_2} = C_{02}\left(V_{GS,M02}^{\phi_2} - V_{OD}\right) \\ Q_{C_{03}}^{\phi_2} = C_{03}\left(V_{SG,M01}^{\phi_1} - V_{OD}\right) \\ Q_{C_{04}}^{\phi_2} = C_{04}\left(V_{GS,M02}^{\phi_2} - V_{OD}\right) \end{cases} \tag{5.7}$$

Applying charge conservation principle, we obtain

$$\begin{cases} Q_{C_{01}}^{\phi_1} + Q_{C_{03}}^{\phi_1} = Q_{C_{01}}^{\phi_2} + Q_{C_{03}}^{\phi_2} \\ Q_{C_{02}}^{\phi_1} + Q_{C_{04}}^{\phi_1} = Q_{C_{02}}^{\phi_2} + Q_{C_{04}}^{\phi_2} \end{cases} \tag{5.8}$$

Using Equation (5.6) and (5.7) in (5.8) and after simplification we, then, get

$$\begin{cases} C_{01}V_{SG,M01}^{\phi_2} + C_{03}\left(V_{SG,M01}^{\phi_2} - V_{SG,M01}^{\phi_1}\right) = C_{01}\left(V_A + V_{OD} - V_{CMI}\right) \\ C_{02}V_{GS,M02}^{\phi_2} + C_{04}\left(V_{GS,M02}^{\phi_2} - V_{GS,M02}^{\phi_1}\right) = C_{02}\left(V_B + V_{OD} - V_{CMI}\right) \end{cases} \tag{5.9}$$

In steady-state conditions, $V_{SG,M01}^{\phi_2} = V_{SG,M01}^{\phi_1} = V_{SG,M01}$ and $V_{GS,M02}^{\phi_2} = V_{GS,M02}^{\phi_1} = V_{GS,M02}$. Since the closed-loop amplifier sets the current in M01 and M02 as equal, and the input bias signal $V_{OD}$ is forced to $V_{CMI}$; from (5.9), it appears that the gate-voltages of M01 and M02 are respectively forced to $V_A$ and $V_B$.

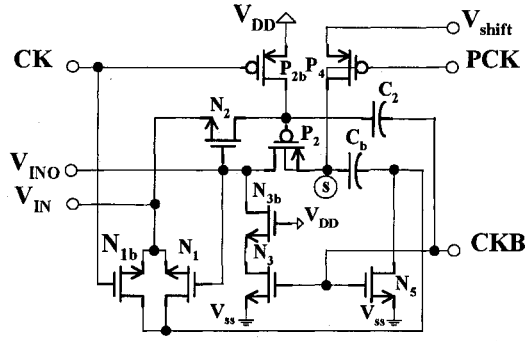
The input common-mode, $V_{CMI}$, was set to half of the supply voltage to achieve the maximum input overdrive, while capacitors $C_{03}$ and $C_{04}$ were set larger than the gate-source capacitances of M01 and M02 to avoid signal attenuation at the gate nodes of M01 and M02.

### *5.1.4 Input level shifter circuit alternative implementation*

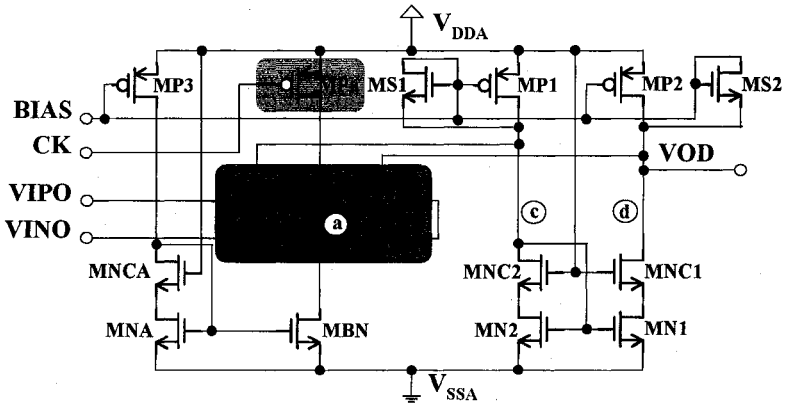
Another possibility is to perform the level shifter circuit using nMOS switch as depicted in Figure 5.5a. The implementation makes use of the generalized nMOS bootstrapped switch method. A linear relation exists between the input signal and level shifter output and is given by:

$$V_{INO} = V_{IN} + V_{shift} \tag{5.10}$$

The related nMOS differential pair is shown in Figure 5.5b. The functionality of the circuit is similar to the pMOS implementation and the same output stage configuration can also be used.




(a)




(b)

**Figure 5.5:** Alternative implementation of low-voltage CMOS opamp: (a) nMOS level shifter, (b) Low-voltage nMOS input stage.

## 5.2 Low-voltage rail-to-rail input analog comparator design

Widespread interest in "affordable-anywhere-anytime" wireless communication and computation has created a critical need for low-power low-voltage analog and digital integrated circuits. Not only do we want our systems to run faster, but we also

want them to run on little or no power. This means increasing the speed and performance of all the components in a system while staying within a restrictive power budget. The demand for higher bandwidth, smaller supply voltage and lower power consumption is also driven by the increasing complexity of electronic equipment. To be able to integrate more functions and more complex functions on a single integrated circuit, the minimum feature size continues to reduce, forcing smaller supply voltages. However the threshold voltage does not scale down proportional to the supply voltage. This introduces many new challenges in designing low-voltage or low-power circuits that meet speed, accuracy, and noise requirements [TRA92].

Comparators are the second most widely used electronic components, after operational amplifiers. They have always been, and are still, an important building block in electronic systems including oscillators, data converters and other front-end signal processing applications. A critical design aspect for comparators is good trade-off between sensitivity, speed, and power consumption. Speed, in fact, can usually be increased at the expense of a higher power consumption, while sensitivity requires high gain and hence low bias current, which leads to a slower time response.

The objective here is to explain the implementation of two analog comparators suitable for low-voltage rail-to-rail input applications.

### *5.2.1 Complementary nMOS/pMOS differential input based comparators*

To optimize the performance of a comparator, one has to consider the resolution, speed and power dissipation trade-off (in a situation of reasonable devices size, i.e.

offset considerations). To achieve high resolution, large gain structures are necessary. Attempting to achieve this with one power-efficient gain stage results in reduced bandwidth due to amplifier gain-bandwidth trade-off. Conversely, medium-speed operation can be obtained by cascading several lower-gain stages at the expense of higher power dissipation. Although individual stages can be made fast, signals require time to propagate through all stages. Possibly the most power-efficient high-speed design method involves combining a low-gain (high-bandwidth) stage with a positive feedback track-and-latch circuit. In essence, this achieves a large nonlinear gain with a high-speed and low power design. Such an approach is illustrated in Figure 5.6. It consists of three main stages: a biasing circuit, a constant-gm rail-to-rail low-gain amplifier stage and a summing-regenerative latch circuit. The input differential voltage is converted into a differential current using the constant-gm stage. This differential current is then summed and fed to the latch circuit for a decision. Details of each stage are described below. The bulk of all pMOS (nMOS) devices in those circuits are connected to the positive (ground) supply voltage $V_{DDA}$ ($V_{SSA}$) unless otherwise stated.

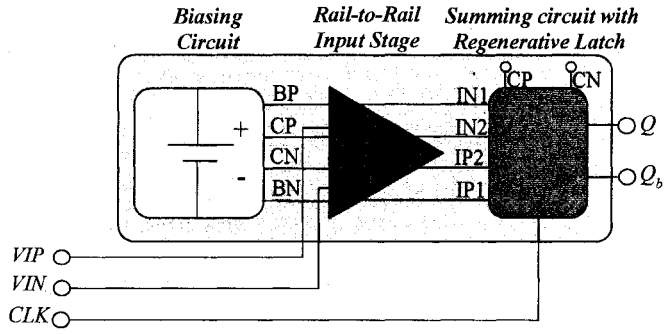



**Figure 5.6:** Comparator Circuit block diagram.

#### *5.2.1.1 Biasing circuit*

The biasing circuit is shown in Figure 5.7. It is a high swing cascode version of the β-multiplier reference of [VIT77]. This circuit utilizes positive feedback and is stable as long as the loop gain is less than unity, which is the case when k > 1 (with k defined as the aspect ratio of transistor MN2 over the aspect ratio of transistor MN1). The biasing current I is defined by the resistance value R and the aspect ratio k using the first-order approximation relation described in [BAK98]. Assuming that transistors MN1 and MN2 are operating in their saturation regions, the current I is given as:

$$I = \frac{2}{R^2 \beta}\left(1 - \sqrt{\frac{1}{k}}\right)^2 \tag{5.11}$$

where $\beta = \left(\mu C_{ox}\frac{W}{L}\right)_{MN1}$.

The minimum supply voltage to guarantee operation in the saturation region is given by

$$V_{DD,\min} = \max\left(V_{th,n} + 3V_{DS,sat}, \left|V_{th,p}\right| + 3V_{DS,sat}\right) \tag{5.12}$$

The typical value of this voltage is around 1.2-V assuming a saturation voltage, $V_{DS,sat}$, of 200 mV with devices mean threshold of 0.5 V (0.18um CMOS).

For ultra low-voltage (1-V and below), the transistors are operating in subthreshold region and hence, the current I becomes:

$$I = n\frac{V_T}{R}\ln k \tag{5.13}$$

where $V_T$ is the thermal voltage (26 mV at room temperature) and n, the subthreshold slope factor, typically approximated to 1 [VIT77].

Unfortunately this circuit has a second stable operating point where all the currents are zero. To guarantee that it does not happen, we have added a start-up circuit that only affects the operation if all the currents are zero at start-up. The biasing current I is affected by the value of the resistance R. A variation of about ± 20% in the resistance value leads to an approximately ±25% in the biasing current. This induced variation in the biasing current has a direct influence on the comparator resolution by means of the differential input stage gain. A typical loss of 3 bits of resolution has been observed.

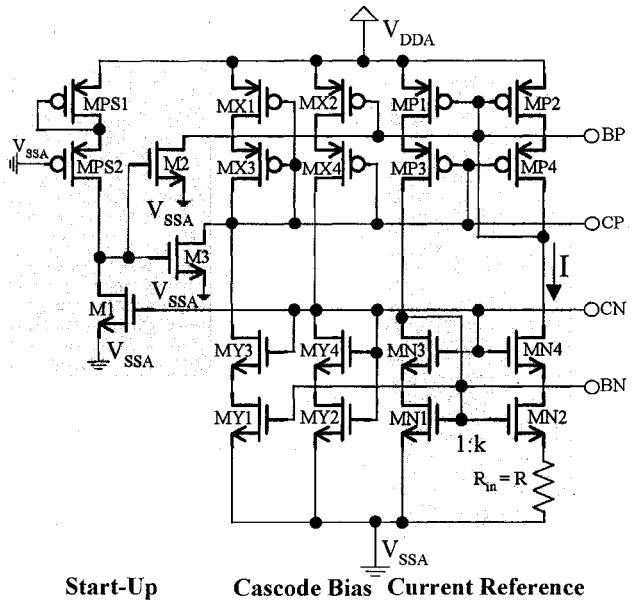



**Figure 5.7:** Comparator biasing circuit.

### *5.2.1.2 Constant-gm rail-to-rail input stage*

Figure 5.8 shows the constant-gm rail-to-rail input stage in a high-swing cascode configuration. When a single differential pair is used as an input stage for a comparator,

a small input common-mode range is obtained. A well-known technique to realize a rail-to-rail input stage is to place two complementary pairs in parallel. When the common mode input signal is close to the rails, only one of the pairs (MP1-MP2 or MN1-MN2) turns on while the other one is cut off. At the mid range, both the n- and p- type pairs operate causing the total transconductance not to constant across the input common mode range and the delay of the comparator to vary as seen in [CHU99]. The transconductance has twice the $g_m$ value of a single pair, assuming both pairs have the same $g_m$. This is an undesirable situation because it gives delay and performance evaluation problems. An easy way to measure and control the transconductance is to tune the biasing currents of the n- and p-type pairs. The complementary input stage with three to one current mirror proposed in [COB95] has been used. The relation describing the way the current is distributed in the differential constant-gm input pair is well described in [COB95], [SAN99] and will not be reported here.

For input stages operated in strong inversion, constant $g_m$, is maintained if the following equations is satisfied:

$$\sqrt{\beta_n I_n} + \sqrt{\beta_p I_p} = \text{constant} \tag{5.14}$$

where $\beta_n = \left(\mu C_{ox} \frac{W}{L}\right)_{MN1,MN2}$, $\beta_p = \left(\mu C_{ox} \frac{W}{L}\right)_{MP1,MP2}$ and $I_n$, $I_p$ are the bias currents for the n-type and p-type differentials pairs, respectively.

Offset on this constant-gm differential operational transconductance amplifier will lead to an offset in the comparator circuit. This offset is mainly due to mismatch and

threshold variation in the input drivers (n and p-type). At the mid-range, when both n- and p-type pairs operate, total offset is the average value of the induced offset from each pair. When the common mode input signal is close to the rails, offset contribution would be the maximum contribution coming from both input pairs. Equations describing those offsets are given below in section 5.2.1.4.

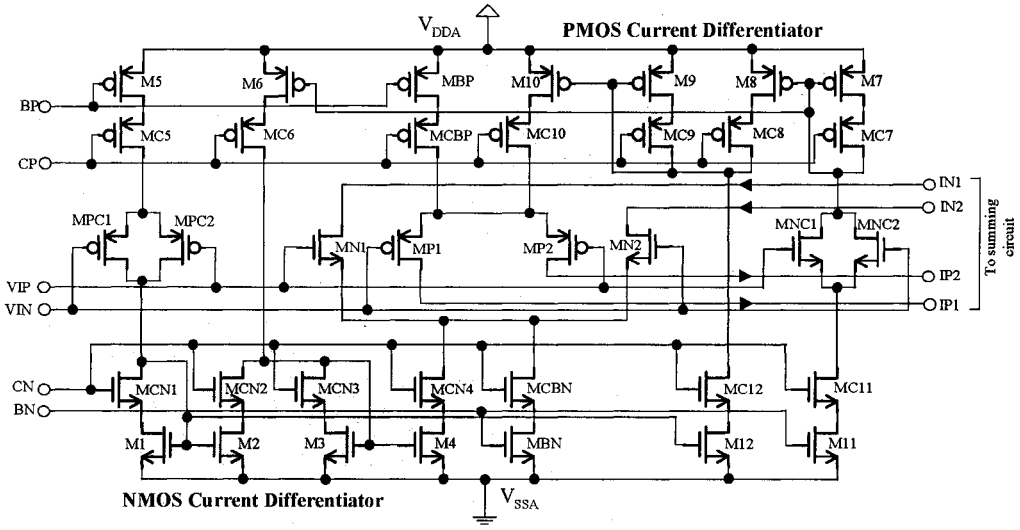



**Figure 5.8:** Constant-gm rail-to-rail comparator input stage.

### *5.2.1.3 Regenerative latch*

The regenerative output latch is based on an approach proposed in [YUK85] and is shown in Figure 5.9, together with the current summing circuit. The latch consists of discharge transistors (M6-M7), an n-channel flip-flop (M1Y-M2Y) with a pair of n-channel transmission gates for strobing (MS1-MS2), p-channel flip-flop (M2X-M3X), and p-channel pre-charge transistors (M1X-M4X). The flip-flop output is taken at the

drain terminals of MS1-MS2 instead of the corresponding source nodes. This is done to increase the regeneration speed and reduce the offset [DEE89]. In addition, the strobing transistors isolate the flip-flop from the comparator output nodes, reducing the load on the flip-flop to the gate capacitance of the flip-flop itself. Offsets caused by the channel length fluctuation (during manufacturing), estimated as the main source of offset voltage, is much lower at zero volt substrate bias [ROY88], [SZE98]. Such an effect is estimated to be the main source of offset voltage in the latch. Thus, transistors channel length can be reduced and the flip-flop speed can be made faster.

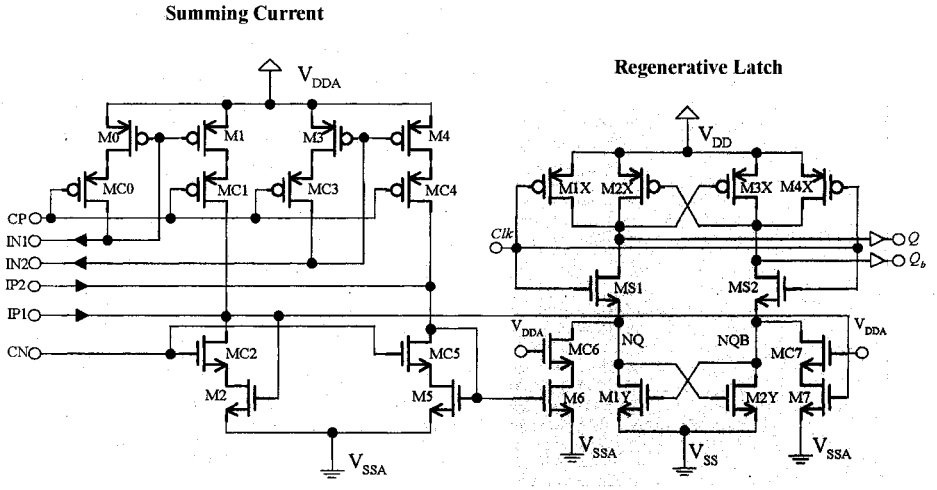



**Figure 5.9:** Summing circuit with regenerative latch.

### *5.2.1.4 Circuit performance*

Our goal is to design a comparator that has high accuracy and high speed with a reasonable transistor size (offset considerations). Before sizing the circuit, we

investigate the main source of offset and what limits the circuit performance. There are two mains source of offset in the circuit and they can be expressed as

$$V_{\text{offset}} = V_{\text{offset, diff pair}} + V_{\text{offset, latch}} \tag{5.15}$$

where $V_{offset,\ diffpair}$ and $V_{offset,\ latch}$ are the offset contribution form the constant-gm differential input pair and the regenerative latch, respectively. The offset voltage in the latch circuit is systematically minimized by the latch topology [ROY88], [SZE98] because the substrate and the source are connected together ($V_{SB}$=0) to the same potential. Also, since the offset voltage in the latch circuit is divided by the differential amplifier gain, which is about 84 V/V in our case, most of the offset sources are in the differential stage.

There are two kinds of offset sources in a MOS differential pair. They are charge density fluctuation, such as surface states and impurity doping concentration, and dimension fluctuation.

Offset associated with the constant gm-input pair consists of contribution from the p- and n-type differential input pairs. Offset contribution of the p-type input pair with n-type load transistor is given by [LAK94]:

$$V_{\text{offset, p-}} = D_p\left(\frac{1}{L_n}+\frac{1}{L_p}\right)\sqrt{\frac{I_p}{2\beta_p}} + \Delta V_{th,p} + \sqrt{\frac{\beta_n}{\beta_p}}\Delta V_{th,n} \tag{5.16}$$

while the one from the n-type input pair with p-type load is

$$V_{\text{offset, n-}} = D_n\left(\frac{1}{L_n}+\frac{1}{L_p}\right)\sqrt{\frac{I_n}{2\beta_n}} + \Delta V_{th,n} + \sqrt{\frac{\beta_p}{\beta_n}}\Delta V_{th,p} \tag{5.17}$$

where $D_p$ and $D_n$ denotes the channel-length imbalance between transistors pairs, for both p-channel and n-channel devices; $L_p$, $I_{bp}$, $\Delta V_{th,p}$ (respectively $L_n$, $I_{bn}$, $\Delta V_{th,n}$) are respectively the channel length, biasing current of the p-type input pair and threshold variation in the p-type devices (respectively the channel length, biasing current of the n-type input pair and threshold variation of the n-type devices). The first term comes from dimension fluctuation in the differential input pair and the load transistors. Using layout techniques, such as common centroid configurations, the transistor mismatch caused by gradients can be greatly reduced. The second and third come from charge fluctuation. Since surface state density and impurity concentration can be well controlled and since the last two terms are proportional to gate oxide thickness (which is small in our case here) these terms are insignificant compared to the first. The first term is increased in inverse proportion to channel length, therefore this term was assumed dominant for the comparator offset consideration.

Numerous works have been performed on offset contribution due to mismatch problems. A useful offset estimation has been reported by Steyaert [STE97] and is given by:

$$\sigma^2(V_{\text{off}}) = \frac{\beta}{g_m L^2}(V_{GS} - V_{th})\left[A_{Vth}^2 + \frac{A_\beta^2}{4}(V_{GS} - V_{th})^2\right] \tag{5.18}$$

where the constants $A_{vT}$ and $A_\beta$ are technology dependent. Table 5.1 from [STE97] summarized the value of those constants for several industrial CMOS technologies.

**Table 5.1:** The matching constants for threshold voltage $A_{Vth}$ and current factor $A_\beta$ for different CMOS technologies.

| Technology | Type | $A_{Vth}$ [mV μm] | $A_\beta$ [% μm] |
|---|---|---|---|
| 2.5 μm | nMOS | 30 | 2.3 |
| [PEL89] | pMOS | 25 | 3.2 |
| 1.2 μm | nMOS | 21 | 1.8 |
| [BAS96] | pMOS | 25 | 4.2 |
| 0.7 μm | nMOS | 13 | 1.9 |
| | pMOS | 22 | 2.8 |

We observe a decrease in those constants with the decrease of the minimum devices sizes. This is mainly due to the decrease in oxide thickness as measured in [PEL97]. The variance reduces with increasing gate area (W/L) and with decreasing oxide thickness. It is clear that for low-offset voltages, the overdrive voltage ($V_{GS}$-$V_{th}$) should be chosen as small as possible. This means in the limit, differential pairs should be designed even in weak inversion. This will, however, severely limits the speed performance of the circuits. For that reason we limit ourselves to transistors in strong inversion. Since we have to select the overdrive voltage as low as possible, the value is best selected at the boundary of strong inversion which is about equal to ($V_{GS}$-$V_{th}$) =200 mV.

Offset voltage dependence on channel fluctuation has been reported in [DEE89], [YUK85]. Based on those results we choose two times the minimum length for p-channel and n-channel input driver transistors and four times the minimum length for the p-channel and n-channel load transistor. In order to achieve high comparison speed the minimum channel has been used in the latch circuit.

### *5.2.2 Regenerative latch-based rail-to-rail comparators*

The novel rail-to-rail low-voltage regenerative latch-based comparator proposed is shown in Figure 5.10. The body of all the pMOS (nMOS) devices in the circuit is connected to the positive (ground) supply voltage $V_{DDA}$ ($V_{SSA}$) unless otherwise stated. The heart of this circuit is a regenerative latch.

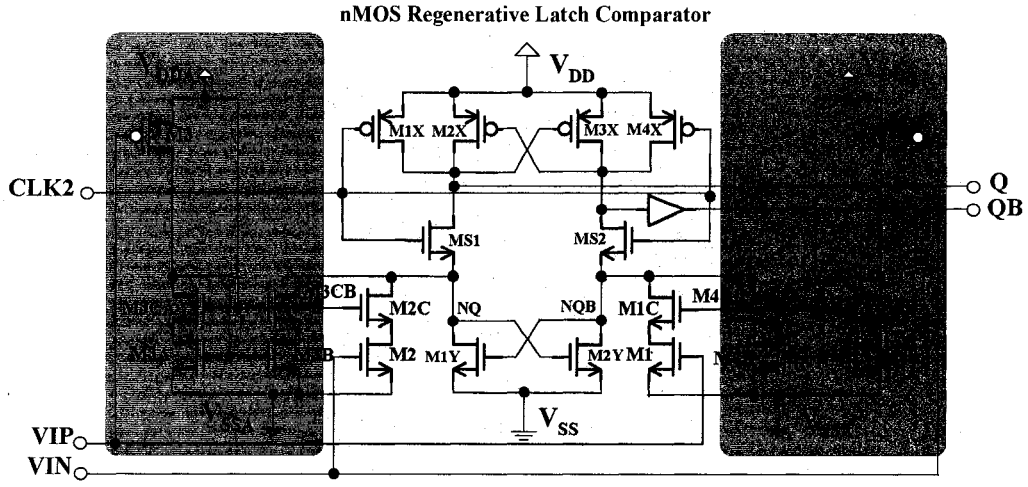



**Figure 5.10:** Low-voltage Rail-to-Rail latch comparator.

The regenerative output latch is similar to the one proposed in [YUK85], which however, has a reduced input range. Transistors (M3, M3A, M3CA, M3B, M3CB) with

(M4, M4A, M4CA, M4B, M4CB) have been added. Their main purpose is to enable the operation of the circuit when the input voltage is close to ground ($V_{SSA}$). A classical NAND-gate based set-reset latch (not shown in the Figure) is connected to the comparator output nodes.

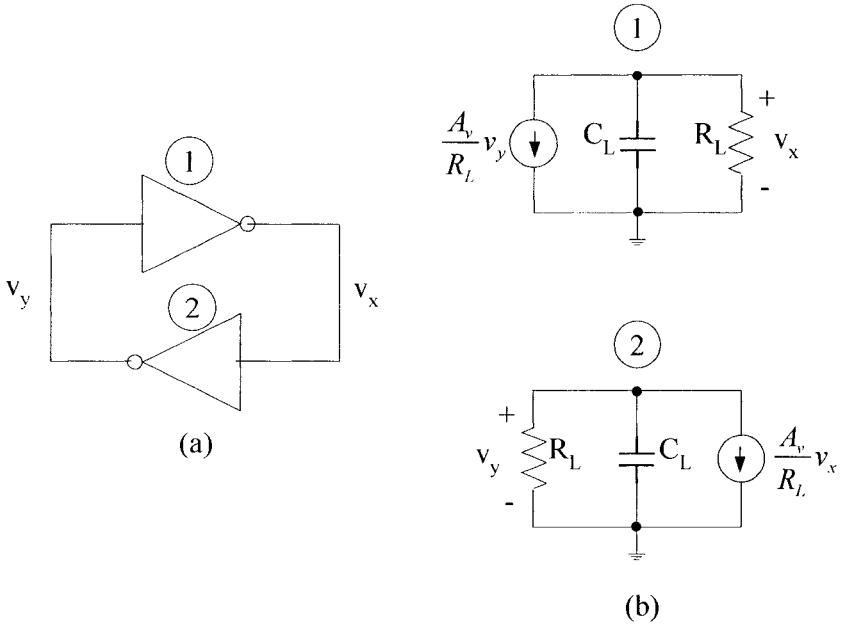



**Figure 5.11:** Track-and-Latch stage: (a) simplified model, (b) linearized model in the latch phase.

The time constant of the latch, during its positive-feedback phase, can be found by analyzing a simplified circuit consisting of two back-to-back inverters, such as those of Figure 5.11a. If we assume that the output voltages of the inverters are closed to each other at the beginning of the latch phase, and the inverters are in their linear range, then each of the inverters can be modeled as a voltage controlled current source driving an

RC load, as shown Figure 5.11b, where Av is the low-frequency gain of each inverter, which has a transconductance given by $G_m = \frac{A_v}{R_L}$. For this linearized model, applying Kirchoff law to the output node, we have:

$$\begin{cases} \frac{A_v}{R_L} v_y = -C_L \left( \frac{dv_x}{dt} \right) - \frac{v_x}{R_L} & \text{inverter 1} \\ \frac{A_v}{R_L} v_x = -C_L \left( \frac{dv_y}{dt} \right) - \frac{v_y}{R_L} & \text{inverter 2} \end{cases} \tag{5.19}$$

Multiplying (5.20) by $R_L$ and rearranging gives

$$\begin{cases} \tau \frac{dv_x}{dt} + v_x = -A_v v_y & \text{inverter 1} \\ \tau \frac{dv_y}{dt} + v_y = -A_v v_x & \text{inverter 2} \end{cases} \tag{5.20}$$

where $\tau = R_L C_L$ is the time constant at the output node of each inverter. Subtracting equation of inverter 1 from the one of inverter 2 gives

$$\frac{\tau}{A_v - 1} \frac{d\Delta V}{dt} = \Delta V \tag{5.21}$$

where $\Delta V = v_x - v_y$ is the voltage difference between the output of the inverters. Solution of (5.21) is given by

$$\Delta V = \Delta V_0 \exp\left(\frac{A_v - 1}{\tau}\right) \tag{5.22}$$

where $\Delta V_0$ is the initial voltage difference at the beginning of the latch phase. Thus, the voltage difference increases exponentially in time with a time constant given by

$$\tau_{ltch} = \frac{\tau}{A_v - 1} \cong \frac{R_L C_L}{A_v} = \frac{C_L}{G_m} \tag{5.23}$$

In the case of MOS devices, normally the output load and the inverter transconductance are proportional to the gate-source capacitance and to the transconductance of a single transistor, respectively. Therefore, Equation (5.23) can be written as

$$\tau_{ltch} = k\frac{L^2}{\mu_n\left(V_{GS} - V_{th,n}\right)} \tag{5.24}$$

where k is a constant which might be between 2 and 4. Note that (5.24) implies that $\tau_{ltch}$ depends primarily on the technology and not on the design (assuming a reasonable design is used that maximizes ($V_{GS}$-$V_{th,\,n}$) and minimizes $C_L$). For a given technology relation (5.24) is very useful in determining a rough estimate for the maximum clock frequency of a latch-and-track comparator. If it is necessary for the voltage difference of $\Delta V_{logic}$ to be obtained for succeeding logic circuitry to safely recognize the correct logic output value, then, by using (5.22), we find (after simplification) the time necessary for this to happen is given by

$$T_{latch} = k\frac{L^2}{\mu_n\left(V_{GS} - V_{th,n}\right)}\ln\frac{\Delta V_{logic}}{\Delta V_0} \tag{5.25}$$

If $\Delta V_0$ is small, this latch time can be large, perhaps larger than the allowed time for the latch phase. Such an occurrence is often referred to as metastability. In other words, because its initial condition value is too small, the difference output voltage of the latch does not increase enough to be recognized as the correct logic value by succeeding circuitry. Even when the initial voltage difference is large enough, it is possible that circuit noise can cause the initial voltage difference to become small enough to cause metastability.

In our design, minimum channel length has been taken for speed optimization.

### *5.2.3 Other low-voltage rail-to-rail analog CMOS comparator*

A simple, high speed, low-voltage and autozeroed comparator circuit is shown in Figure 5.12 [DIN85]. During the sample period ($\Phi_1$), the input signal $V_{IN}$ is sample via $sw_2$ and level shift capacitor C and help on the parasitic gate capacitance of the inverter ($M_1$-$M_2$). Simultaneously, the comparator inverters ($M_1$-$M_2$, $M_3$-$M_4$) are autozeroed to their toggle point by closing $sw_3$ and $sw_4$. This establishes the toggle point, which is the point of highest speed and small signal inverter gain. The comparison process is performed on period $\Phi_2$ and the digital output is latched.

The circuit can operate at very low-voltage (close to the device threshold), however, switches in the circuit need to be implemented using bootstrapped techniques (section 4.1) or be driven by clock booster circuits. Details mathematical expressions are

given in [ENZ87], while optimized design procedure is described in [FOT94], [MAR01]. This recommended low-voltage CMOS comparator has been successfully used by [TRE02] in the design of a CMOS image sensor with pixel analog-to-digital conversion.

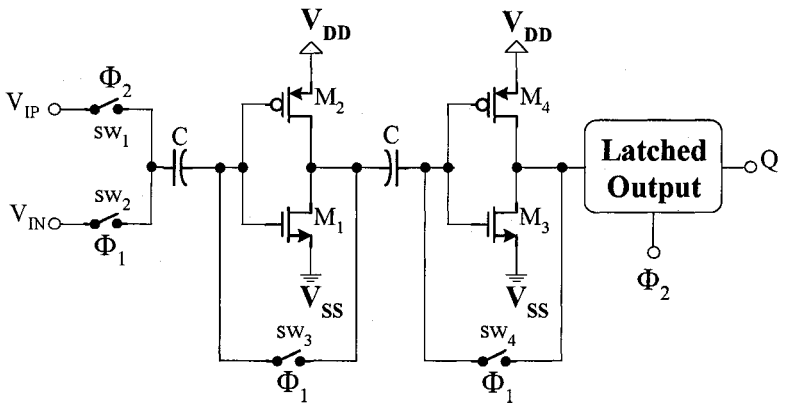



**Figure 5.12:** Low-Voltage high-speed autozeroed comparator.

## 5.3 Low-voltage rail-to-rail successive approximation ADC

We propose and describe here two different and novel design solutions for the very low-voltage rail-to-rail (1-V) successive approximation ADC in a standard 0.18 μm CMOS process. The ADC was designed for medium resolution applications such as data acquisition. The block diagram of the ADC is shown in Figure 5.13. It contains a track-and-hold stage as well as a digital-to-analog converter, a successive-approximation register with control logic and finally a voltage comparator. The major analog and digital building blocks are discussed below.

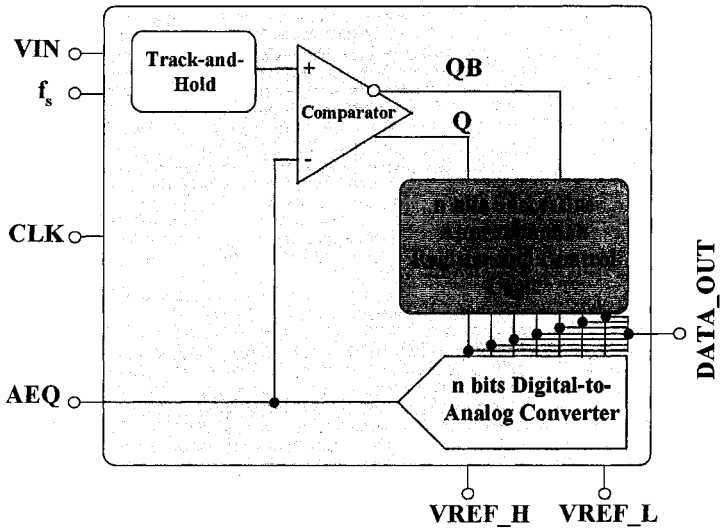



**Figure 5.13:** Block diagram of a successive approximation ADC.

### *5.3.1 Track-and-hold circuit*

Most ADCs typically employ a sample-and-hold (S/H) circuit at the front-end that must achieve high speed, high linearity and high precision with low-power dissipation. This circuit serves as an interface between the ADC's input or the input analog signal to be encoded and the rest of the ADC. The S/H circuit sustains a certain point of an input analog signal for a certain amount of time (i.e. necessary for the rest of the circuit to react on this value).

The most serious factors affecting the performance of a high precision CMOS sample-and-hold circuit are charge injection and clock feedthrough. Several methods have been proposed to overcome these problems. These include the use of a dummy MOS transistor for charge cancellation, a compensation network for offset cancellation,

a closed-loop architecture, a Miller hold capacitance and a switched-opamp based sample-and-hold circuit. Although charge cancellation methods that make use of a dummy transistor produce good simulation results, great care must be exercised when laying out the clock tree controlling the complementary switches. Other methods have either limited input bandwidth or introduce high design complexity. To overcome these limitations we propose a novel track-and-hold circuit based on the dummy compensated bootstrapped switch. Design techniques and considerations as well as experimental results have been described in depth in section 4.2 while Figure 4.8 shows the track-and-hold scheme.

### *5.3.2 Rail-to-rail comparator*

The two analog rail-to-rail input CMOS comparators described in section 5.2 can be used in the proposed ADC implementation. However, due to the specifications (circuit must operate at 1-V or below), only the circuit proposed in section 5.2.2 and shown in Figure 5.9 is a candidate for such implementation. Its operation principle and design methodology are well described in the mentioned section.

### *5.3.3 Successive approximation register and control logic*

The SAR has typically two inputs and two outputs. The first of these inputs is a clock signal that will usually be an input pin to the ADC. This will determine the rate at which the ADC encodes the input analog signal. The second input is the output from the comparator. If this output is high (the DAC output is too low), this tells the SAR to

increase the digital number that it outputs. Vice versa, if this output is too low (the DAC output is too high), this tells the SAR to decrease the digital number that it outputs. The two outputs are a digital output (whose number of bits depend on the specs of the ADC) and a "end of conversion" (EOC) output that is 'true' or 'false' and indicates whether the current digital output data is "data valid".

The SAR of an n-bit ADC contains an n-bit register that is cleared prior to the start of the conversion process. The register bits are set one at a time to a high state and produce an input to the n-bit DAC. The control circuit is essentially a ring-counter. The heart of the SAR and the control logic, in the proposed implementation of Figure 5.4, is a robust single phase clocking D flip-flop circuit [AFG96]. A pMOS static latch in the flip-flop is depicted in Figure 5.14.

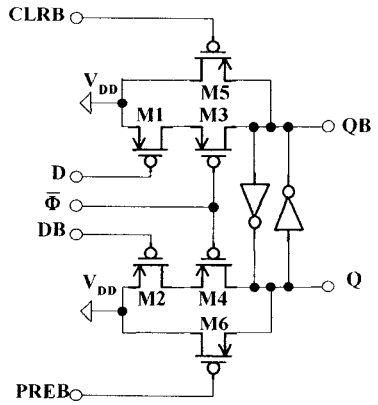



**Figure 5.14:** Low-voltage Latch circuit used in SAR.

True single phase static D flip-flops can be constructed by cascading two latches with different clock polarity and display the minimum transistors count (8) to achieve such functionality. Additional transistors (M5-M6) have been added to achieve the

preset and clear functions usually needed in the implementation of successive approximation A/D. The flip-flop has no limitation on the input clock slope.

### *5.3.4 Digital-to-analog converter circuit*

The DAC is part of the feedback loop inside the ADC. It converts the current digital output (output from SAR) to an analog signal to be used as the second input to the comparator (to be compared with the current analog input signal).

A wide variety of DAC architectures exist, ranging from very simple to complex. Each, of course, has its own merits. Voltage division, current steering and even charge scaling can be used to map the digital value into an analog quantity. However, some of these architectures may not be suitable for low-voltage design. Due to the voltage limitation induced by the transmission gate and capacitance implementation, a charge scaling DAC cannot be used for very low-voltage applications. The use of fringing capacitors [SAM98] and low-voltage, low-stress bootstrapped switches [FAY00b] overcomes these limitations.

Two DAC structures have been used in the proposed ADC and are briefly described below.

#### *5.3.4.1 Voltage mode R-2R DAC*

The first DAC used in our design is the voltage mode R-2R ladder of Figure 5.15. An opamp is not needed since the output voltage goes directly to a high impedance

node. If the output of the DAC needs to drive a low impedance node a voltage follower would be used at the interface.

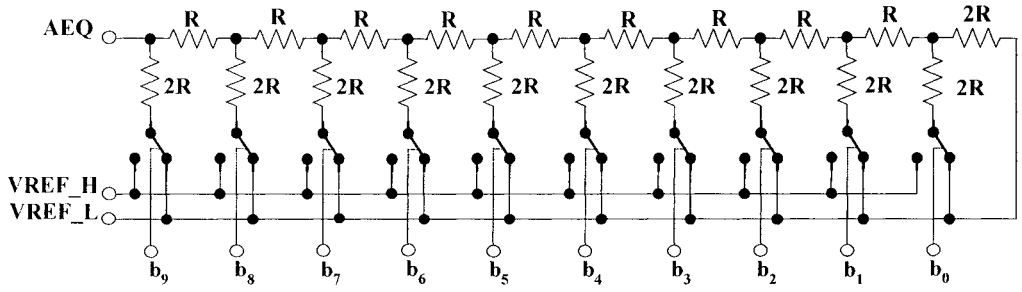



**Figure 5.15:** A 10-bit voltage-mode R-2R DAC.

This configuration presents an advantage compared to a current mode R-2R ladder requiring an output opamp, as the opamp adds noise to the system [CON91]. Generally speaking, the output of an n-bit voltage DAC can be written as

$$V_{AEQ} = V_{REF\_L} + \sum_{k=1}^{k=n} \frac{1}{2^k} \left( b_{n-k} V_{REF\_H} + \overline{b_{n-k}} V_{REF\_L} \right) \tag{5.26}$$

where $V_{REF\_L}$ and $V_{REF\_H}$ are respectively the lower and higher reference voltage applied to the DAC. By using the voltage mode DAC, the problem of limited output swing (due to opamp) associated with the current mode DAC is solved.

The matching between the resistors of the R-2R ladder is one of the most important and limiting factors that determine the linearity (e.g., DNL and INL) of the entire DAC. When designing any type of resistor string DAC, it is helpful to be able to estimate the resistor matching requirements based on a desired resolution.

[BAK02] has shown that the worst case DNL and INL conditions tend to occur at midscale when the code transitions from 01...11 to 10...00, and are respectively given by

$$\begin{cases} DNL = \left[\frac{\Delta R}{R} - \frac{1}{2^n}\right]\left(V_{REF\_H} - V_{REF\_L}\right) \\ INL = \frac{1}{2}\frac{\Delta R}{R + \Delta R}\left(V_{REF\_H} - V_{REF\_L}\right) \end{cases} \tag{5.27}$$

For the DNL and INL to be within 0.5 LSB, the matching required of the resistors is

$$\left|\frac{\Delta R}{R}\right| \leq \frac{3}{2}\frac{1}{2^n} \tag{5.28}$$

For a 10-bit, data converter to have a DNL less than 0.5 LSB requires the MSB resistor to match within 0.05 % of the lower resistors.

Equation (5.27) results in a pessimistic estimate for the matching required of the resistors. The resistance along the string does not vary abruptly at the MSB resistor but rather, in most cases, varies linearly from LSB to MSB. The matching requirement results in a practical limit of 10 bits for a R-2R ladder based converter with no special layout or circuit techniques. This requirement can be relaxed by using a segmented method for the four most significant bits [KEN00].

Another limiting factor of interest is the settling time of the DAC. The DAC must settle within the resolution of the overall converter, for example, ½ LSB. The time constant, $\tau$, associated with the DAC is given by

$$\tau = RC_L \tag{5.29}$$

where R is the ladder resistance and $C_L$, the capacitive load at the output node. $C_L$ is mostly the gate capacitance of the comparator and can be kept small. We can use this time constant to relate the final ideal output voltage, $V_{AEQfinal}$, to the actual output voltage, $V_{AEQ}$, using

$$V_{AEQ} = V_{AEQfinal}\left(1 - \exp\left(-\frac{t}{\tau}\right)\right) \tag{5.30}$$

or, relating this to the required accuracy,

$$1 - \frac{V_{AEQ}}{V_{AEQfinal}} = \exp\left(-\frac{t}{\tau}\right) = \frac{1}{2^{n+1}} \tag{5.31}$$

The requirement settling time is then

$$t_{settling} = (n+1)\tau \ln 2 \tag{5.32}$$

The maximum clock frequency is then estimated as

$$f_{clk,\max} = \frac{1}{t_{settling}} = \frac{1}{(n+1)\tau \ln 2} \tag{5.33}$$

Equation (5.33) shows that the fundamental way increase the operation frequency is to reduce the resistance in the R-2R ladder (assuming we have no control over the load capacitance). However, decreasing the resistance leads to an increase in the overall power dissipation.

Noise is another important design consideration. Noise analysis of the resistor networks entails grounding the digital input bits and placing thermal noise voltage sources in series with each resistor. The value of the spectral density of noise squared of each source is 4×kT times the corresponding resistance, where k is Boltzmann's constant

($1.38\times10^{-23}$ J° $K^{-1}$) and T is the absolute temperature in degrees Kelvin. The equivalent network noise output voltage squared per Hertz, $E_{nA}^2$, is the sum of the individual resistor noise contributions evaluated through the appropriate voltage divider for each noise source. It has been shown [CON91] that

$$E_{nA}^2 = \frac{4kTR}{1+\left(1-\frac{1}{2^{n-1}}\right)} \tag{5.34}$$

As n increases, $E_{nA}^2$ rapidly approaches the value of 2kTR. The RMS squared value of the quantization noise is given as [BAK02]

$$E_{Q_e}^2 = \frac{\Delta^2}{12} = \frac{1}{12}\left(\frac{V_{REF\_H} - V_{REF\_L}}{2^n}\right)^2 \tag{5.35}$$

In a rail-to-rail design ($V_{REF\_L} = 0$, $V_{REF\_H} = V_{DD}$), this tends to become

$$E_{Q_e}^2 = \frac{V_{DD}^2}{12\times 2^{2n}} \tag{5.36}$$

Taking into account the fact that quantization noise must dominate over the network noise leads to

$$R \le \frac{2-\frac{1}{2^{n-1}}}{4kT}\frac{V_{DD}^2}{12\times 2^{2n}} \tag{5.37}$$

For a 10-bit, rail-to-rail voltage mode converter, operating under $V_{DD} = 1$, this condition becomes $R \le 9.81\times10^{12}\ \Omega$ !!!. It is clear that network noise is not really a limiting factor when sizing a R-2R voltage mode ladder. The resizing has to be done for optimal power dissipation and settling time.

Table 5.2 below shows the various characteristics of resistor available in a submicron CMOS process.

**Table 5.2:** Properties of resistors in a submicron CMOS process [BAK02].

| Silicided | Resistor Type | Rs (ohms/sq) AVG. | TCR1 (ppm/C) AVG. | TCR2 (ppm/C$^2$) AVG. | VCR1 (ppm/V) AVG. | VCR2 (ppm/V$^2$) AVG. | Mis-match % |
|---|---|---|---|---|---|---|---|
| | n-well | 500 ± 10 | 2400 ± 50 | 7 ± 0.5 | 8000 ± 250 | 500 ± 50 | < 0.1 |
| | n+ poly | 120 ± 1 | 21 ± 10 | 0.6 ± 0.03 | 700 ± 50 | 150 ± 15 | < 0.5 |
| | p+ poly | 300 ± 5 | 160 ± 10 | 0.8 ± 0.03 | 600 ± 50 | 150 ± 15 | < 0.2 |
| | n+ diff | 100 ± 2 | 1500 ± 10 | 0.04 ± 0.1 | 2500 ± 50 | 350 ± 20 | < 0.4 |
| | p+ diff | 125 ± 3 | 1400 ± 20 | 0.4 ± 0.1 | 80 ± 80 | 100 ± 25 | < 0.6 |
| * | n+ poly | 3 ± 0.3 | 3300 ± 90 | 1.0 ± 0.2 | 2500 ± 125 | 3800 ± 400 | < 0.4 |
| * | p+ poly | 2 ± 0.1 | 3600 ± 50 | 1.0 ± 0.2 | 2500 ± 400 | 5500 ± 250 | < 0.7 |
| * | n+ diff | 3 ± 0.1 | 3700 ± 50 | 1.0 ± 0.2 | 350 ± 150 | 600 ± 60 | < 1.0 |
| * | p+ diff | 2.5 ± 0.1 | 3800 ± 40 | 1.0 ± 0.2 | 150 ± 50 | 800 ± 40 | < 1.0 |

At a glance, it may appear as though the n-well offers the best choice for a resistor in a data converter since it has < 0.1 % matching characteristic. However, after reviewing the voltage coefficient specification, a problem seems to arise. A tradeoff has to be made when choosing the resistor material used in the design of a data converter based on a R-2R ladder. In general, the resistor's width and length should be at least 10 and 100 times the minimum feature size of the process, respectively. Minimum width and length for the resistors is required both for matching and to ensure that the self-heating, which occurs because of the different current densities flowing in the R-2R resistors, does not cause any noticeable differences in DAC linearity [BAK02]. In

simple terms, the larger resistor area dissipates heat better than the same valued resistor in a smaller area.

### *5.3.4.2 pMOS-only current mode R-2R DAC*

Figure 5.16 below is a pMOS-only R-2R ladder DAC based on a linear current division principle [BUL92] (see appendix A). Transistors in Figure 5.16 have the same aspect ratio (W/L). Both transistors M1 and M2 have the same gate voltage $V_{biasp}$.

The input current, $I_{ref}$, flowing towards node $X_9$ is divided equally into two currents $I_{ref}/2$ between M1 and M2 [BUL92]. This current is flowing through one of the pMOS transistors M2A or M2B, depending on b9 being logic 0 or logic 1. The current entering node $X_8$ has the same value $I_{ref}/2$ and is equally divided in 2, as $I_{ref}/4$. Again, this current is flowing through one of the pMOS transistors M4A or M4B and so forth. The current value of $I_{ref}/2^9$ will enter node $X_0$ and will be divided having the value $I_{ref}/2^{10}$Hence the general expression for the current as:

$$I_k = I_{ref} \times 2^{-(n-k)} b_k \tag{5.38}$$

where $I_k$ is the current value after being divided at node $X_k$ and $b_k$ is the gate voltage of the pMOS transistors, either logic 0 or logic 1.

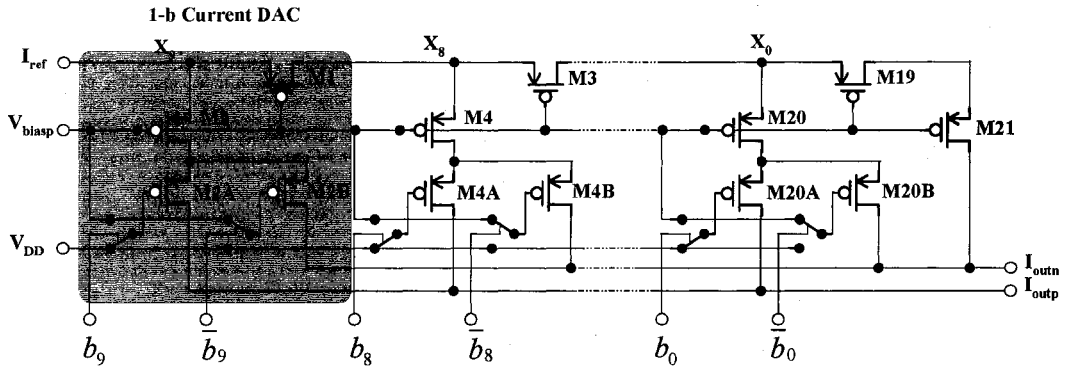



**Figure 5.16:** MOSFET-only current DAC.

The $I_k$ values contribute to the output currents $I_{outn}$ and $I_{outp}$ given as:

$$\begin{cases} I_{outp} = I_{ref} \sum_{k=1}^{k=10} 2^{-k} b_{n-k} \\ I_{outn} = I_{ref} \sum_{k=1}^{k=10} 2^{-k} \overline{b}_{n-k} \end{cases} \tag{5.38}$$

where *n* the number of bits (n=10, here) of the pMOS-based current mode.

The statistical design of a similar DAC (10-bit resolution) using nMOS transistor network has been carried out by Tuna [TAR01]. The quantitative measure of the effects of mismatch between transistors in the circuit is provided with the optimization process.

The output voltage requirement dictates the choice of pMOS over nMOS. The resolution of this DAC can be very high without trimming as reported in [HAM98] and scales with technology. However, it requires a low-voltage current-to-voltage converter. The class AB rail-to-rail input/output opamp of Figure 5.17 is used with a resistor in a negative feedback configuration to realize this function. It is a modified version of the CMOS push-pull opamp proposed by Masua [MAS84] for a 5-V operating system.

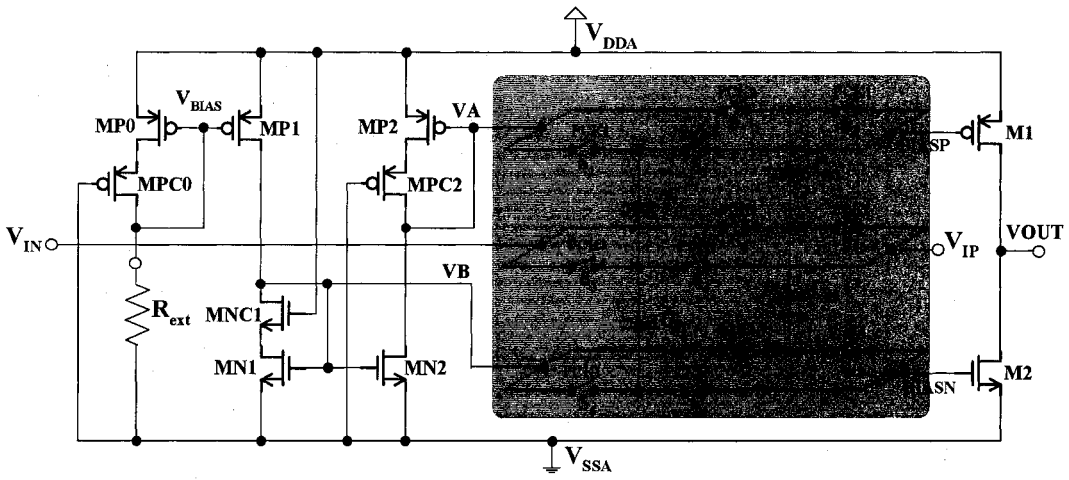
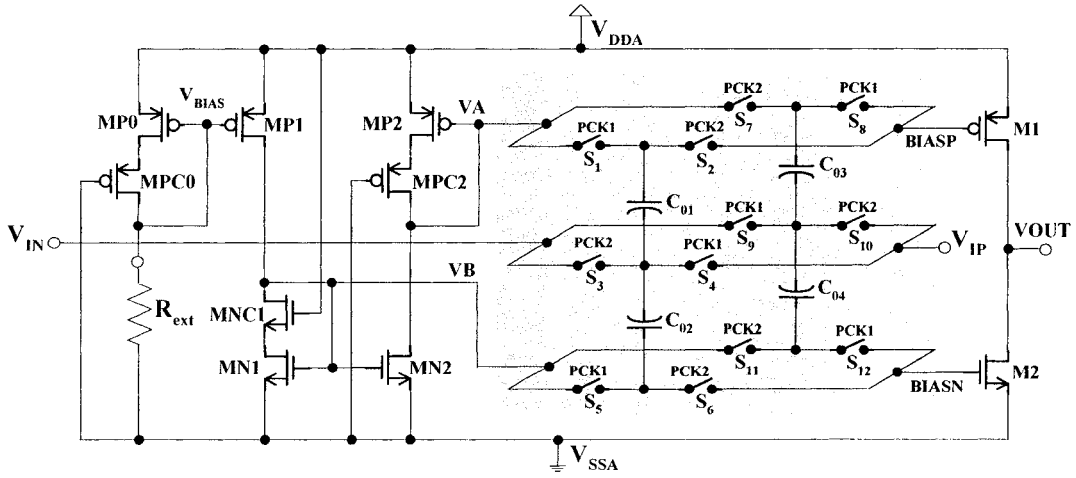



**Figure 5.17:** Low-voltage opamp used for current-to-voltage conversion.

The principle of operation of this opamp is similar to the one of class-AB output stage described in section 5.1.3. nMOS switches driven by a clock signal booster [FAY00b] are used in the circuit to enable the operation at low-voltage. These switches can also be implemented using a pMOS bootstrapped arrangement [FAY00b]. If space constraints are concerned, only the input switches (S3-S4, S9-S10) need to be implemented using the bootstrapped method.

A depth description of the state-of-the-art techniques and methodologies used to design analog opamp and analog CMOS comparators, digital-to-analog in submicron process has bee given in this chapter. A detailed description of an experimental successive approximation ADC has been also provided with matching requirements, settling time and noise analysis. The following chapter will focus on the experimental and simulation results of the proposed circuits.

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# *Chapter 6*

# *RESULTS AND DISCUSSION*

*"I was born not knowing and have only had a little time to change that here and there."*
*- Richard P. Feynman*

Following the design of the low-voltage circuit techniques described in the previous chapters, simulation and experimental characterization process have been performed on most of the proposed circuits. However, long term reliability and performance under stress condition characterization was not performed. This chapter describes and presents the experimental results.

## 6.1 Technology and test setup

The implementation of the described analog building blocks has been simulated with Hspice using BSIMv3 and a 0.18 μm n-well digital CMOS technology. The mean value threshold voltages are approximately 0.5 V and – 0.6 V for nMOS and pMOS transistors, respectively. In the 0.18 μm CMOS process, metal-metal are used in the implementation of capacitors because of the non-availability of poly-poly capacitors. The bootstrapped switch based sample-and-hold experimental prototype was fabricated with the same process.

Clocks and single frequency sinusoidal input signals were generated using

Hewlett Packard HP81130A pulse and HP33120A arbitrary waveform generators, respectively. Chip output signals were observed using Tektronix analog and digital oscilloscopes TDS320 and TDS7154.

## 6.2 Experimental results of the bootstrapped switch based sample-and-hold

In the design of the CMOS analog switch suitable for high precision sample-and-hold circuit three, main goals have been set:

- nearly constant ON-resistance (Equation 4.5);
- clock feedthrough voltage linearly related to the input signal (Equation 4.8) with an almost constant charge injection (Equation 4.6);
- and the low induced distortion level.

The circuit performance will be tested with respect to those criteria.

### *6.2.1 Layout*

The reliability of the circuit can be further improved by carefully laying out some of the critical devices. Although the relative voltages between gate, source, and drain do not exceed $V_{DD}$, the drain-to-substrate and source-to-substrate voltages of some devices exceed $V_{DD}$ (assuming an n-well process). Devices $N_{b2}$ (Figure 4.5b) and $N_2$ with $P_{5b}$ (Figure 4.6c) are subject to this large voltage. Thus, for improved reliability, the drain of devices $N_{b2}$ (Figure 4.5b) and $N_2$ with $P_{5b}$ (Figure 4.6c) should be laid out circularly. The "doughnut" transistor structure also has the advantage of being area-efficient with less parasitic capacitance at the drain; making this structure attractive for

high-speed applications. The layout of an nMOS doughnut transistor $N_{b2}$ with the gate surrounding the drain is illustrated in Figure 6.1.

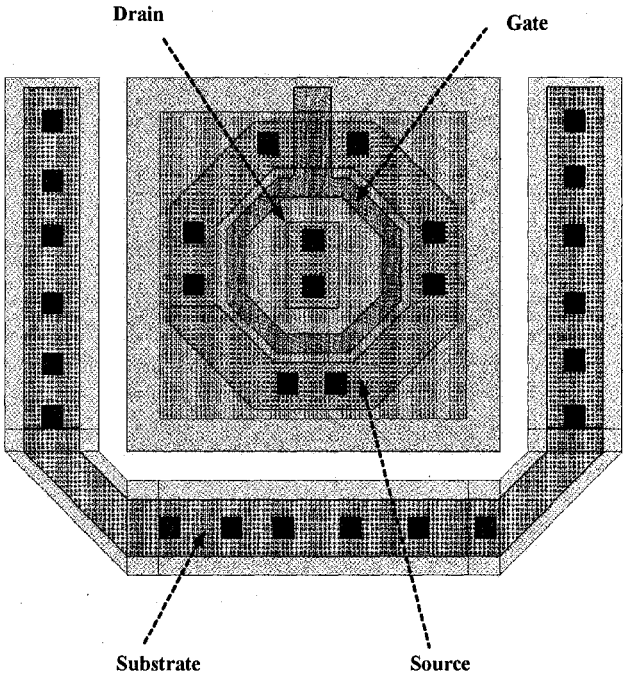


**Figure 6.1:** Physical layout of an nMOS doughnut transistor $N_{b2}$.

The lateral spacing of the metal layers shrinks with scaling while the thickness of the metal layers and the vertical spacing of the metal layers stay relatively constant. This effect has been used in the capacitor implementation. A layout of a typical 2-pF capacitor is depicted in Figure 6.2. Only two metal layers (M3-M4) have been used. The

capacitor occupied 90x55 $\mu m^2$.

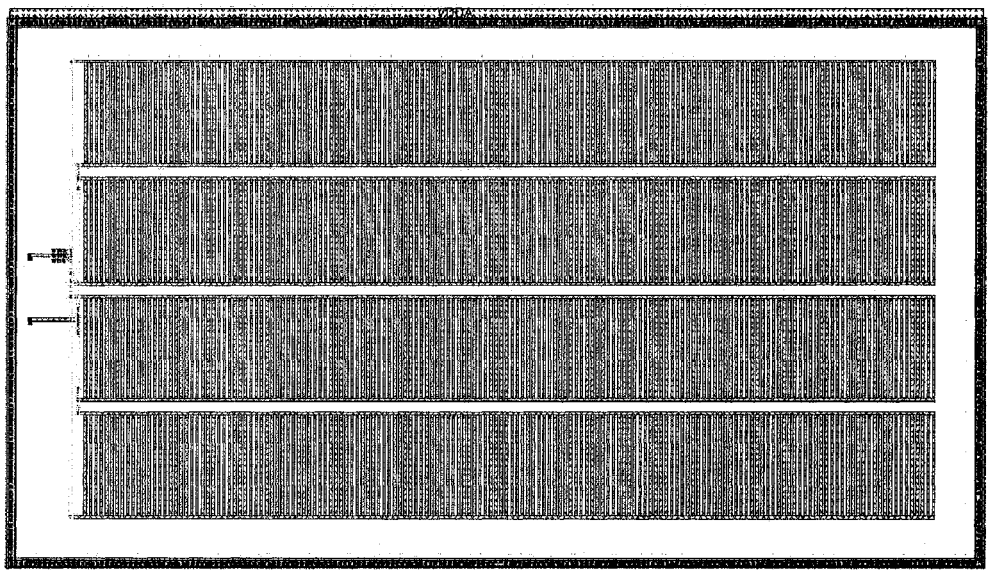

**Figure 6.2:** Physical layout of a 2 pF fringing effects based metal-metal capacitors.

### *6.2.2 Switch ON-resistance*

The ON-resistance has been tested for different supply voltages ranging from 0.65 to 1.6 V and compared with the simulation results. The test setup circuit is shown in Figure 6.2. The test procedure is described as follows:

a. Set the supply voltage at a constant level (e.g. $V_{DD}$ = 1.6 V);

b. Set the input voltage at $V_{IN}$ = 0.1 V;

c. Measure the output $V_{OUT}$ using a digital multimeter;

d. Compute the current flowing through the switch using the following equation:

$$I_{ON\_SW} = \frac{V_{OUT}}{R_L} \tag{6.1}$$

e. Compute the switch ON-resistance corresponding to this input level using relation (6.2) below:

$$R_{ON\_SW} = \frac{V_{IN} - V_{OUT}}{I_{ON\_SW}} \tag{6.2}$$

f. Continue to compute the $R_{ON\_SW}$ for other values of $V_{IN}$ up to the set value of $V_{DD}$;

g. Run the test procedure for different values of $V_{DD}$.

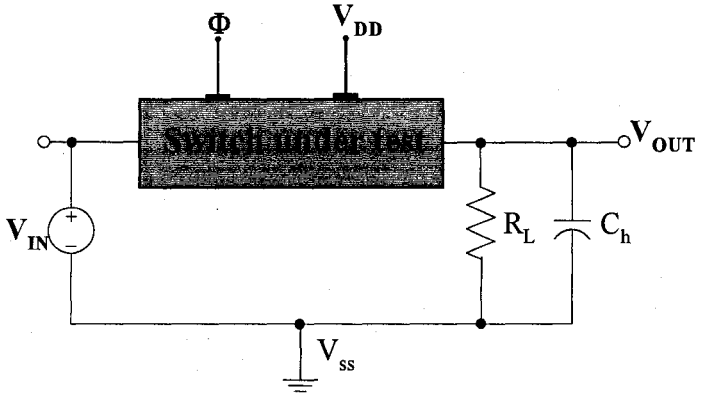


**Figure 6.3:** Switch ON-resistance test setup.

The value of $R_L$ has been established around 1 MΩ. However, an arbitrary value can be selected with negligible impact on the obtained results. Typical value for $C_h$ is around 5 pF. Capacitor $C_h$ is used to discharge the output when clock signal Φ is low.

Figure 6.4 presents the results of a comparison between the simulated ON-

resistance and the measurement results under a 1.6 V operating supply voltage. Similar results are presented in Figures 6.5 and 6.6 for 1.0 and 0.65 V operating supply voltage conditions, respectively. Under a 0.65 V operating condition, a typical variation of 0.38 Ω is observed for input signal varying from 0.125 V to 0.65 V.

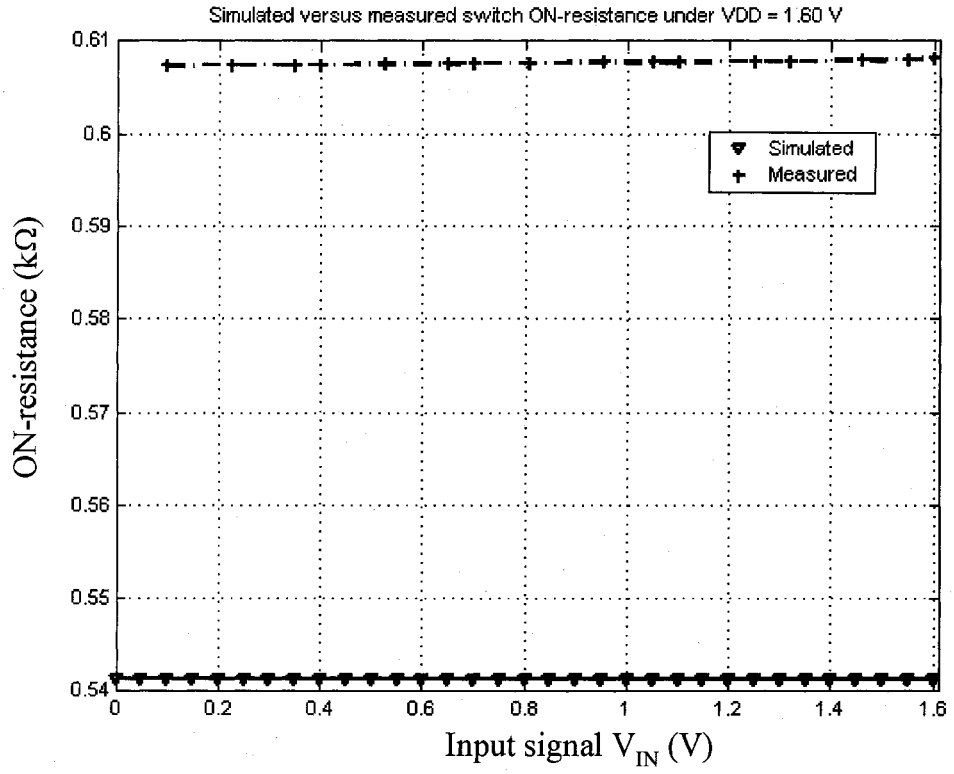


**Figure 6.4:** Comparison between simulated and measured switch ON-resistance variations at 1.60 V supply voltage.

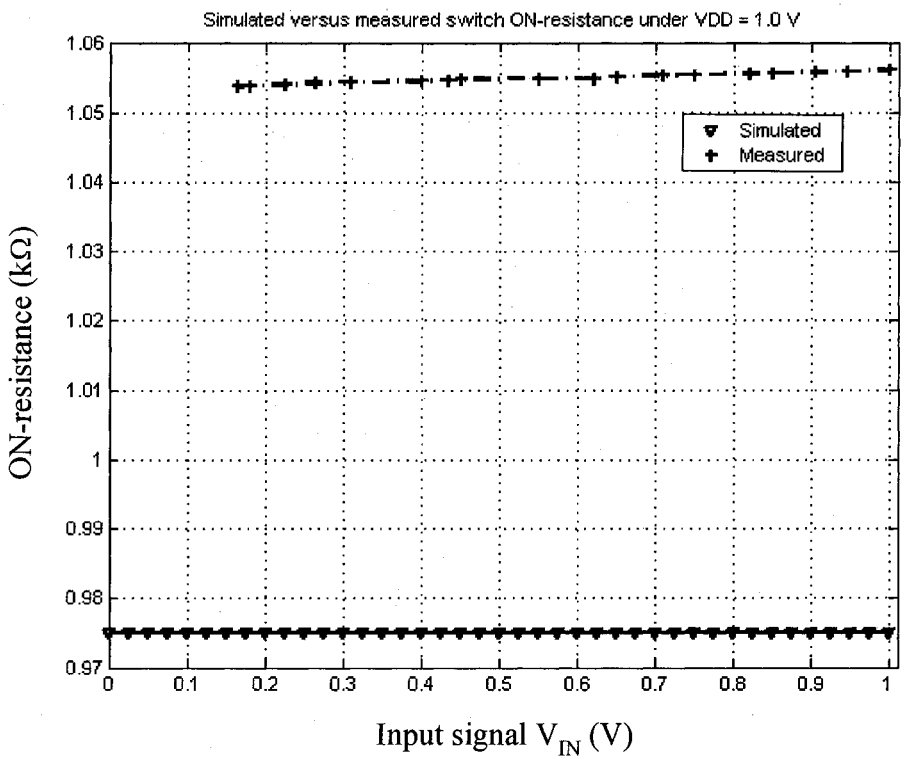


**Figure 6.5:** Comparison between simulated and measured switch ON-resistance variations at 1.0 V supply voltage.

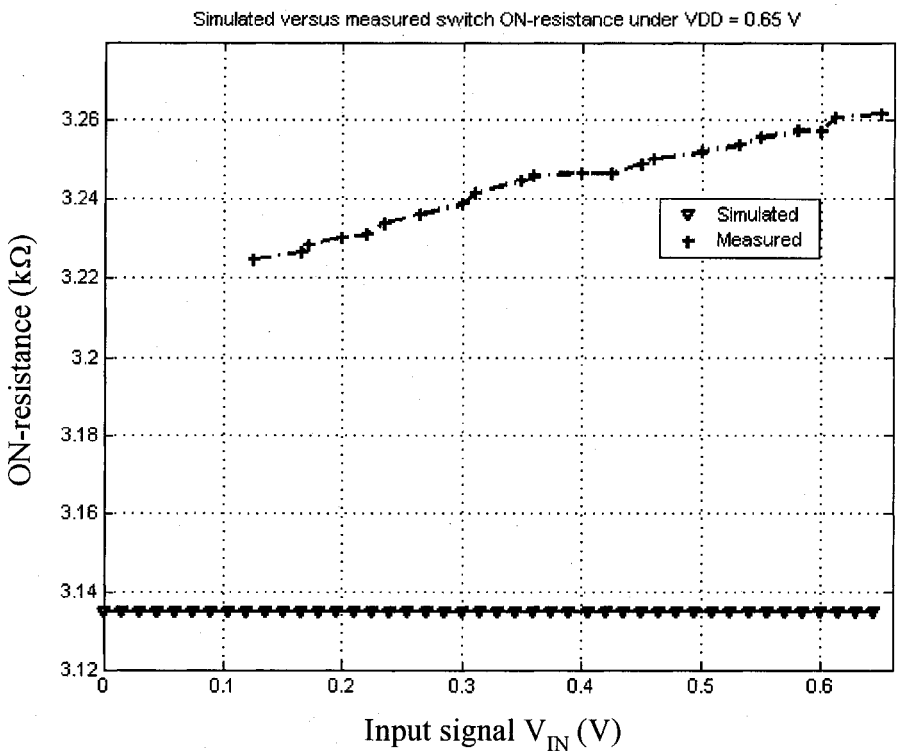


**Figure 6.6:** Comparison between simulated and measured switch ON-resistance variations at 0.65 V supply voltage.

The plot in Figure 6.7 is the mean value of ON-conductance variation with respect to the supply voltage. An almost linear variation is observed, which is in concordance with relation (4.5). The deviation $\Delta R/R$ is plotted in Figure 6.8 with respect to the supply voltage. At high supply voltage a small variation is observed.

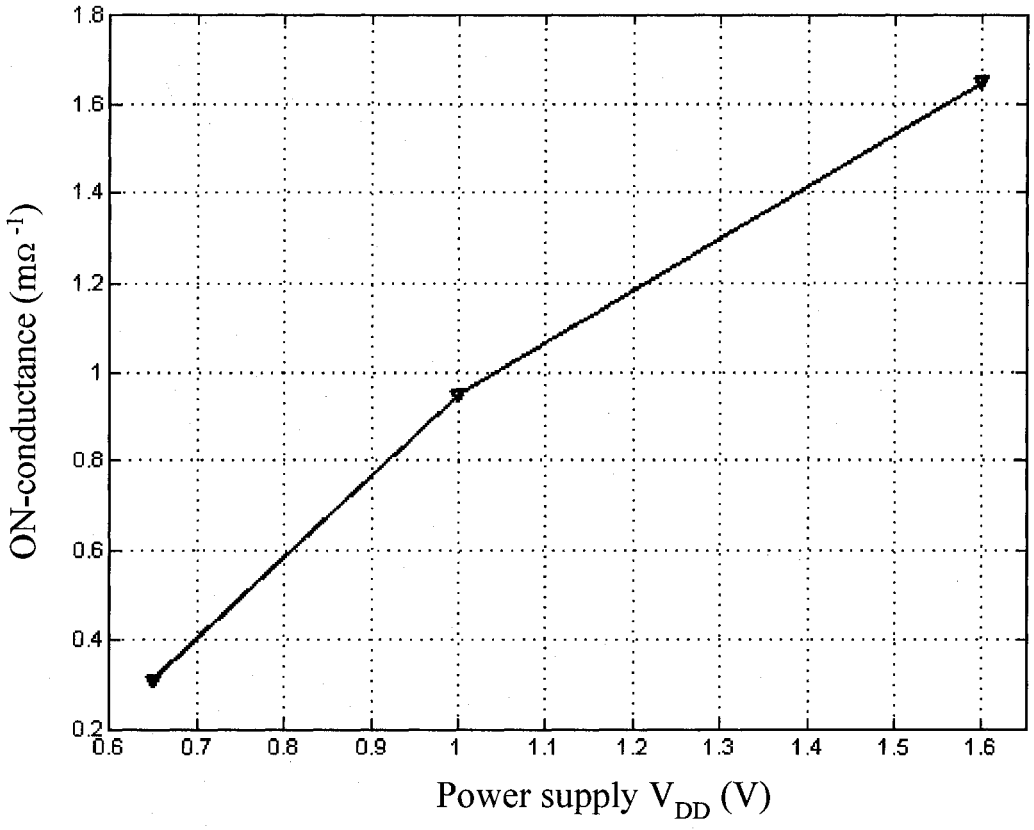


**Figure 6.7:** Measured switch ON-conductance variation with respect to supply voltage.

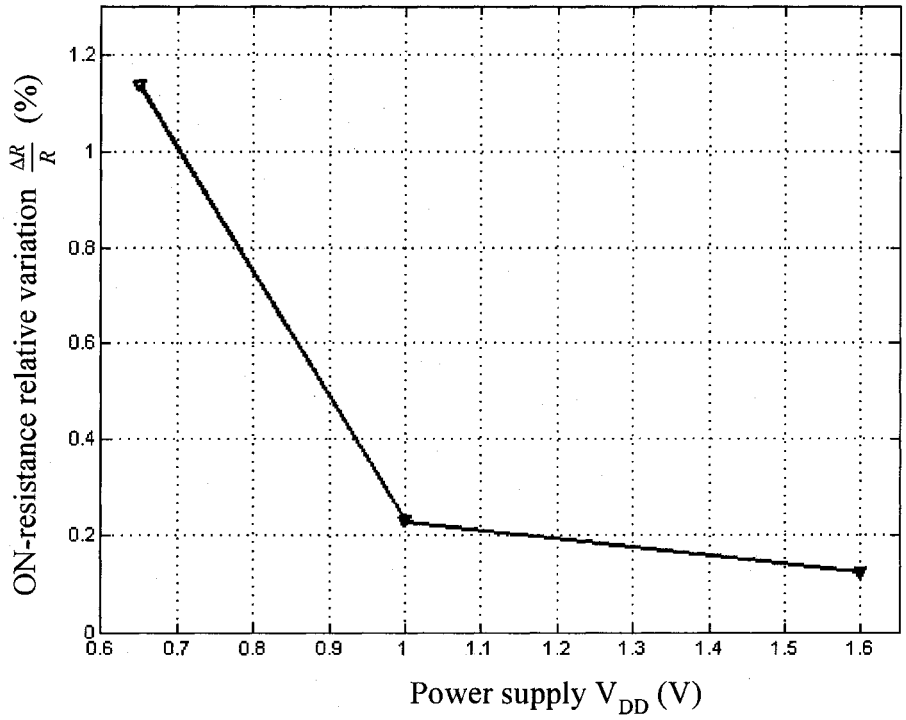


**Figure 6.8:** Measured relative switch ON-resistance variation with respect to supply voltage.

### *6.2.3 Clock feedthrough error voltage test*

The test setup circuit presented in Figure 6.9 has been used to test the clock feedthrough induced error voltage. The basic measurement procedure (Figure 6.10) starts by switching clock signal Φ to $V_{DD}$, which turns the switch on. The load capacitance is charged to its initial value called the analog voltage $V_{OUT1}$. The clock signal Φ is turned to $V_{SS}$ thus, turning the switch off.

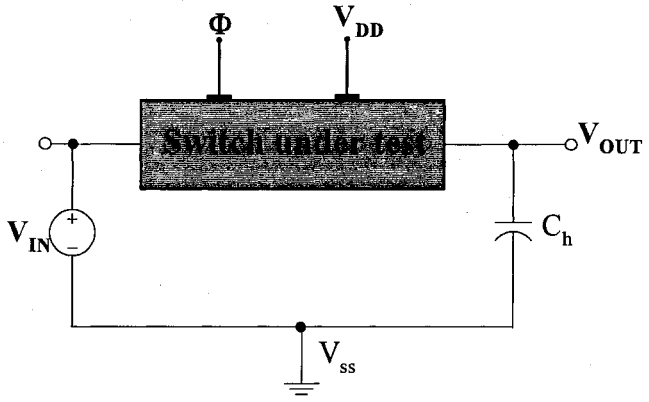


**Figure 6.9:** Basic circuit used in measuring clock induced error voltage.

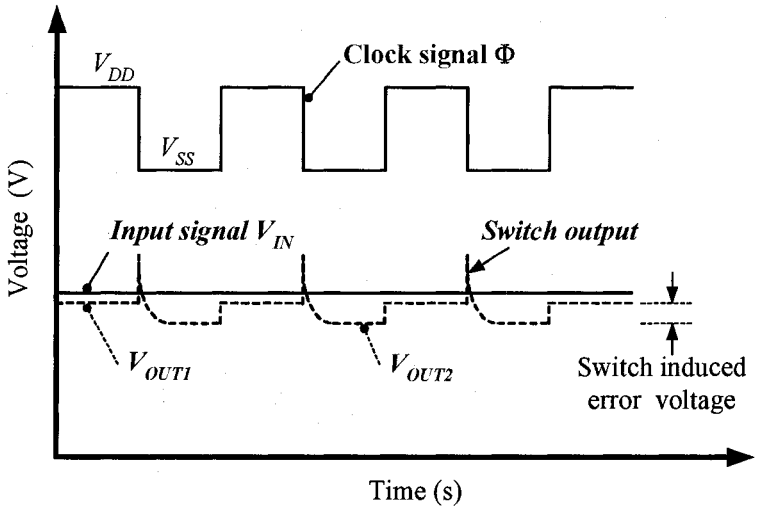


**Figure 6.10:** Basic switch induced error voltage measurement procedure.

The output voltage of the switch becomes $V_{OUT2}$. The difference between the measured output voltage before and after the gate transition yields the feedthrough voltage at the output node. The measurement was performed for different input voltage

levels with supply voltage equal to 0.65 V and 1.0 V. A 1 MHz clock signal frequency has been selected. The value of $V_{OUT1}$ and $V_{OUT2}$ is estimated as the mean of the 256 samples taken when the switch is ON or OFF, respectively.

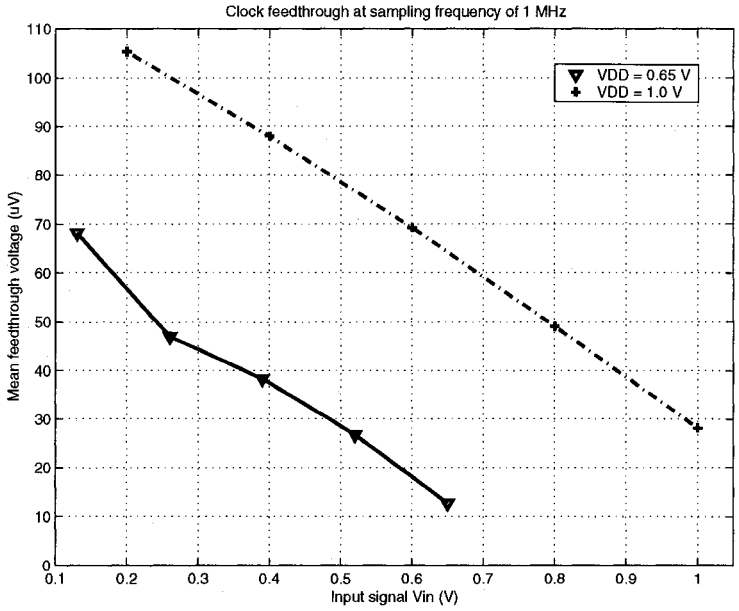


**Figure 6.11:** Measured dependence of the feedthrough voltage on the analog input.

Figure 6.11 above presents the dependence of the feedthrough error voltage with respect to the analog input. An almost linear variation is observed. This result is in concordance with relation (4.8). The dummy compensation mechanism removes the charge injection contribution from the observed voltage error. Even if this charge injection is not completely removed, it has been demonstrated that it is signal-independent (Equation 4.6) and thus appears as a constant offset at the output.

### *6.2.4 Linearity and switch-induced distortion test*

One of the most useful techniques for evaluating the dynamic performance of sample-and-hold circuit is coherent sampling, a method that increases the spectral resolution of an FFT and eliminates the need for window sampling when certain conditions are met [ROB95], [BUR01]. Coherent sampling describes the sampling of a periodic signal, where an integer number of its cycles fits into a predefined sampling window. Mathematically, this can be expressed as:

$$\frac{f_{IN}}{f_S} = \frac{M}{N} \tag{6.3}$$

where $f_{IN}$ is periodic input signal, $f_S$ the sampling/clock frequency of the device under test, M an integer number of cycles within the sampling window and N, the number of data points in the sampling window or FFT. If M is a prime number and the relation (6.3) holds, then the samples within the unit time interval are unique. In other words, this coherence ensures that the location of the N samples is controlled and repeatable. N is typically chosen to be a power of two to accommodate fast Fourier transform (FFT) algorithm. The application of the coherency principle makes testing of switches more efficient and reliable by simplifying the analysis of the spectral resulting from the FFT. Thus, the dynamic performance such as signal-to-noise ratio (SNR) and total harmonic distortion (THD) can be tested [GRO97].

Measured waveform of Figure 6.12 shows the circuit performing sample-and-hold operation (sampling speed of 0.25 MHz at an input frequency of 34.179 kHz) of an

input signal amplitude of 1 V under a supply voltage of $V_{DD}$ = 1 V. Figure 6.13 presents the results for the same parameters with an input signal and using a supply voltage $V_{DD}$ of 0.65 V.

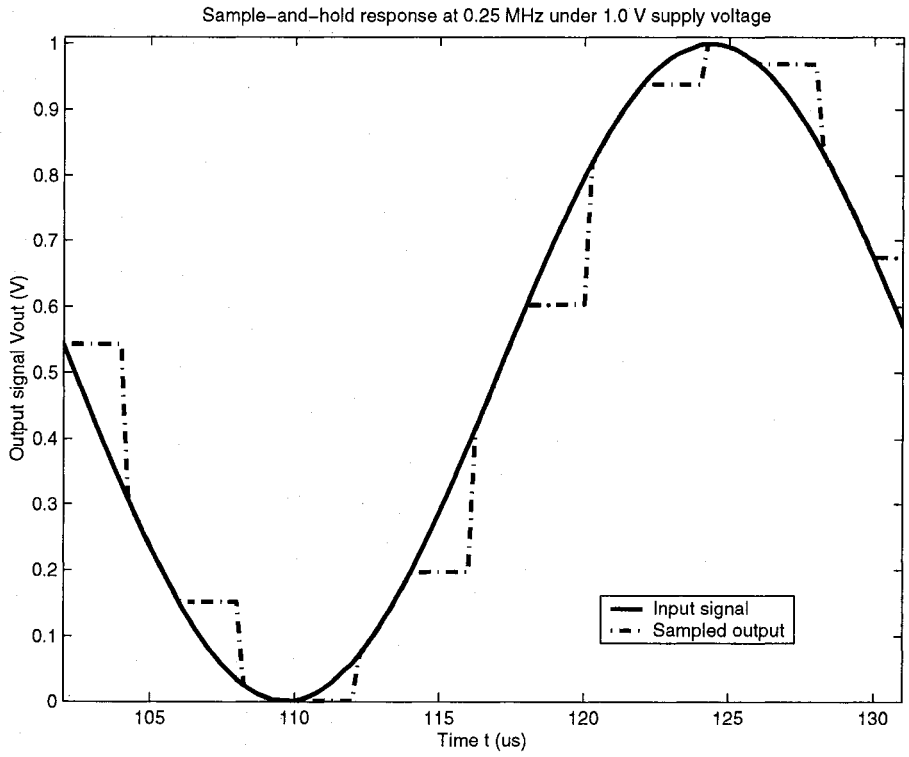


**Figure 6.12:** Measured input/output of the bootstrapped switch circuit test chip with a sampling speed of 0.25 MHz, an input frequency of 34.179 kHz and a signal amplitude of 1 $V_{PP}$ under $V_{DD}$ = 1 V.

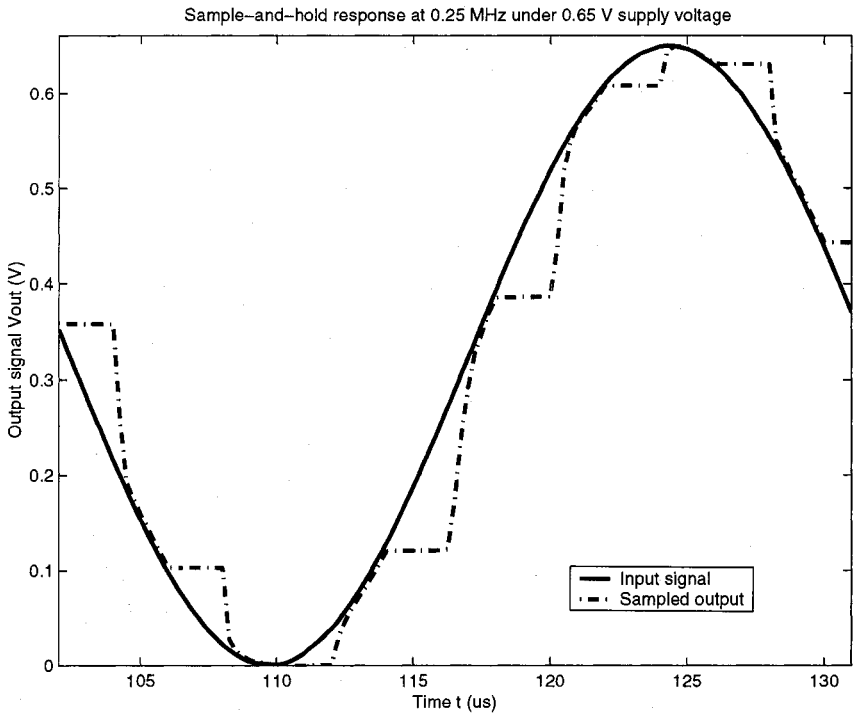


**Figure 6.13:** Measured input/output of the bootstrapped switch circuit test chip with a sampling speed of 0.25 MHz, an input frequency of 34.179 kHz and a signal amplitude of 0.65 $V_{PP}$ under $V_{DD}$ = 0.65 V.

Direct photographies of the measured waveform with the Tektronix oscilloscope TDS320 have been reported in Figures 4.22 and 4.23 when the circuit operates at a sampling speed of 0.5 MHz with a sinusoidal input signal frequency of 82.03 kHz.

To further evaluate the non-linearity, we generated the power spectral density (PSD) of the sample-and-hold output signal via Matlab. A spectrum analyzer connected to the output node can also be used. A total of N = 256 ($2^8$) data samples were used with

35 signal cycles to ensure the coherency sampling requirement (Equation 6.3). Figures 6.14 and 6.15 show the spectrum of the sampled-and-hold waveform under sampling frequency of 0.25 MHz. The measured SINAD obtained for a supply voltage of about 1.0 and 0.65 V is 71.0527 dB and 45.775 dB, respectively. This corresponds to an effective resolution of 11.5 bits and 7.3 bits, respectively.

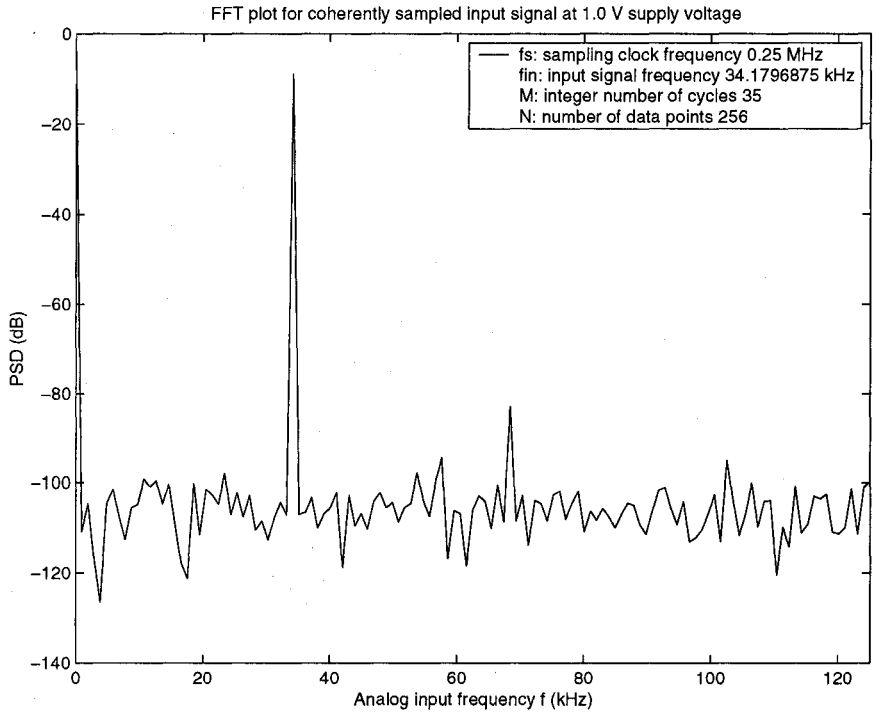


**Figure 6.14:** Measured spectrum of the bootstrapped switch-based sample-and-hold circuit test chip with a sampling speed of 0.25 MHz, an input frequency of 34.179 kHz and a signal amplitude of 1 $V_{PP}$ under a supply voltage $V_{DD}$ = 1 V.

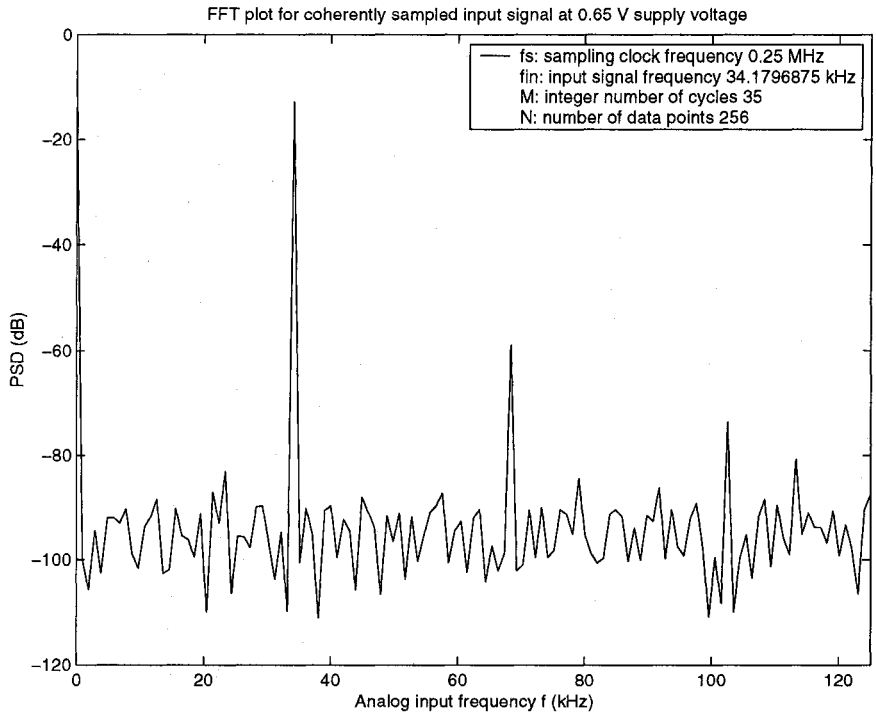


**Figure 6.15:** Measured spectrum of the bootstrapped switch-based sample-and-hold circuit test chip with a sampling speed of 0.25 MHz, an input frequency of 34.179 kHz and a signal amplitude of 0.65 $V_{PP}$ under a supply voltage $V_{DD}$ = 0.65 V.

The measured spurious free dynamic range (SFDR) versus the input signal amplitude at the 0.25 MHz and 1 MHz clock rates are represented in Figures 6.16 and 6.17 for supply voltage of 1.0 V and 0.65 V, respectively. The spectrum dependence on the switch peak-to-peak input signal voltage is quite linear at 0.25 MHz. The same dependence is observed at 1 MHz with small signal amplitude. The performance degradation observed

above 0.35 $V_{PP}$ at 1 MHz sampling frequency under 0.65 V is mainly due to the transmission gate formed by transistors $N_2$ and $P_2$ (Figure 4.6). The ON-conductance of this transmission gate becomes high and considerably increases the settling time of the input-dependent control signal g at the gate of transistor $P_0$. Overall performance is great for single pMOS based sample-and-hold circuit compared to previously reported design operating at 3.3 V supply voltage [MOO03], [SUZ02], [KOB01], [WAL99].

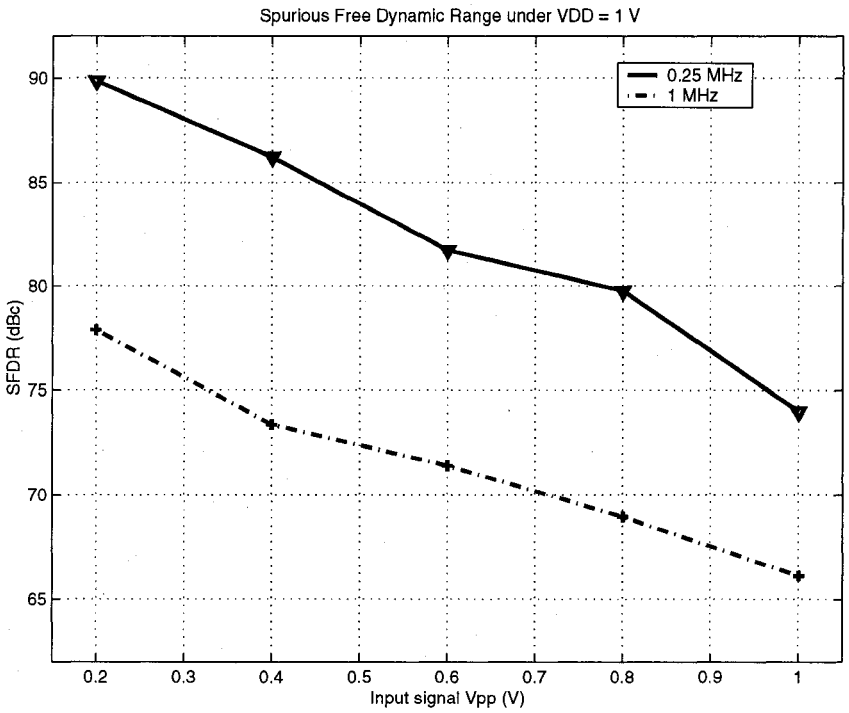


**Figure 6.16:** Measured SFDR versus input level under a supply voltage $V_{DD}$ = 1.0 V.

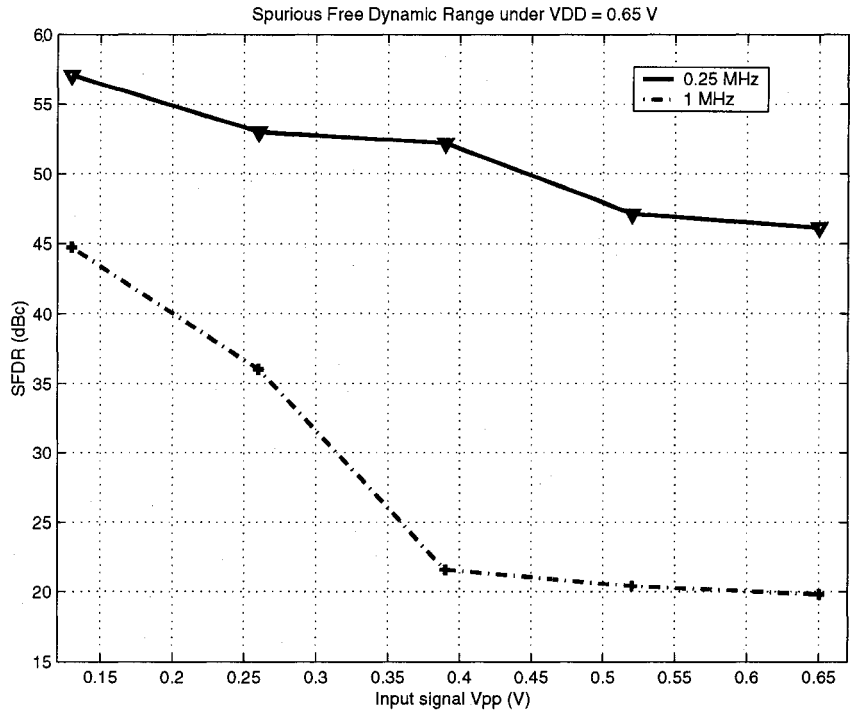


**Figure 6.17:** Measured SFDR versus input level under a supply voltage $V_{DD}$ = 0.65 V.

## 6.3 Simulation results

This section presents the simulation results of the additional proposed analog buildings (comparators and opamp) with the functional simulation of the experimental 10-bit successive approximation ADC.

### *6.3.1 Complementary nMOS/pMOS differential input based comparators*

Comparator circuit of Figure 5.6 has been simulated and analyzed with respect to $g_m$ variation, propagation delay (settling time) and input common-mode range.

Figure 6.18 shows the sum of the square roots of the tail currents of the complementary differential amplifiers used in the amplifier stage as a function of the input common-mode voltage. Although the appropriate transistor scale factor is not included, it serves as a useful measure of how the amplifier $g_m$ varies with the input common-mode voltage. Here we see that the sum of the square roots of currents varies between 4 and 4.7 $mA^{0.5}$. A peak occurs at each end of the input common-mode voltage range, corresponding to the condition when one differential pair is partially on while the other pair is fully on. For the device sizes chosen in our design, this corresponds to a 14% change in $g_m$ over the full range of common-mode input voltage, as predicted by the formula provided in [COB95]. The simulated comparator performance using $V_{DD}$ = 1.65 V with a switching voltage overdrive of ± 0.2014 mV (which corresponds to a ± 0.5 LSB of a 12 bit precision) and an inverter load (which is the case in our application) is summarized in table 6.1. The propagation delay shows little variation, and the delay in all cases remains smaller than 1 ns. The propagation delay, when the common-mode input value is near one of the power supply voltage, is only slightly increased above this value.

The propagation delay in Table 6.1, which has been simulated under static conditions ($V_{IP}$ and $V_{IN}$ are set to a DC input level with an overdrive of ± 0.2014 mV), is less than 1ns. Worst-case driving condition waveform of a comparator described in Figure 6.19 has been used to perform additional simulation under dynamic conditions. Results show an average propagation delay of about 15 ns. This is due to the speed

limitation of both the nMOS and pMOS current differentiators (highlighted in Figure 5.8). This can be improved at the price of increasing the current level.

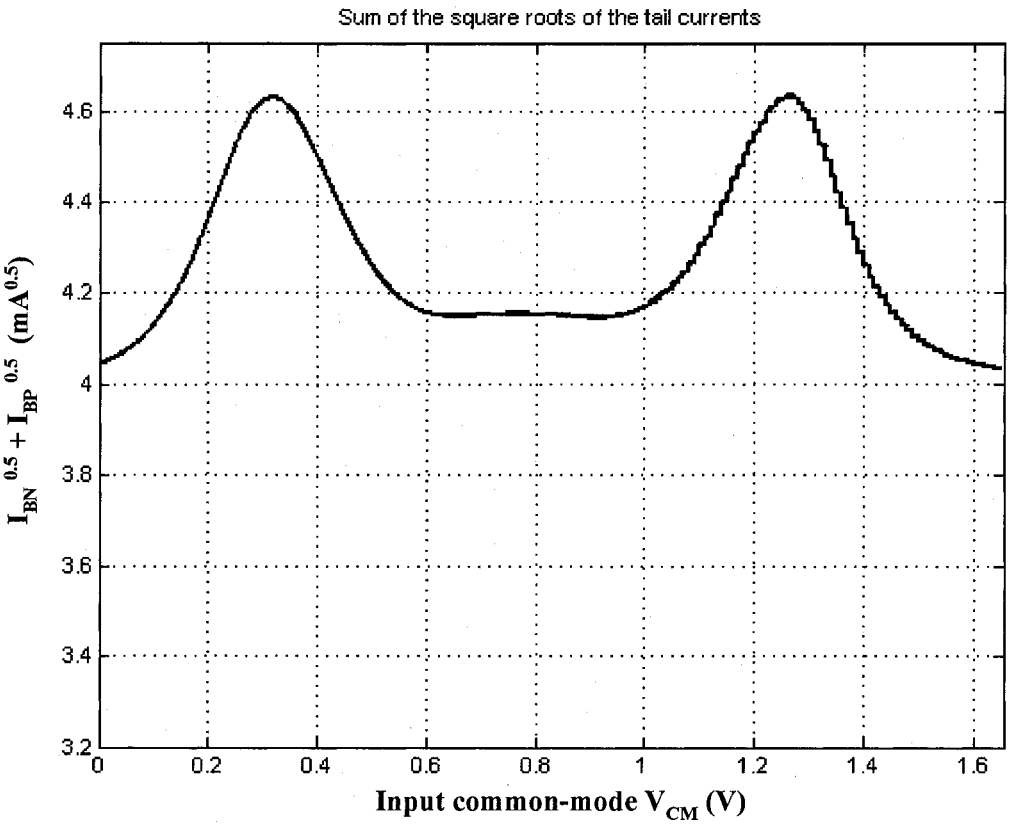


**Figure 6.18:** Simulated variation of the sum of the square roots of the tail currents proportional to $g_m$.

**Table 6.1:** Summary of comparator simulation results.

| | | | | |
|---|---|---|---|---|
| 0.00 | 46.766 | 35.398 | 679.360 | 88.499 |
| 0.10 | 46.329 | 35.399 | 619.320 | 88.486 |
| 0.20 | 42.858 | 35.413 | 408.820 | 88.381 |
| 0.30 | 41.976 | 35.420 | 430.570 | 88.319 |
| 0.40 | 41.822 | 35.421 | 437.320 | 88.312 |
| 0.50 | 41.888 | 35.421 | 436.710 | 88.312 |
| 0.60 | 41.831 | 35.421 | 435.310 | 88.313 |
| 0.70 | 42.103 | 35.418 | 414.830 | 88.332 |
| 0.80 | 44.530 | 35.405 | 448.940 | 88.445 |
| 0.90 | 46.705 | 35.499 | 623.440 | 88.491 |
| 1.00 | 46.807 | 35.399 | 695.400 | 88.492 |
| **AVERAGE** | 43.965 | 35.419 | 511.820 | 88.398 |

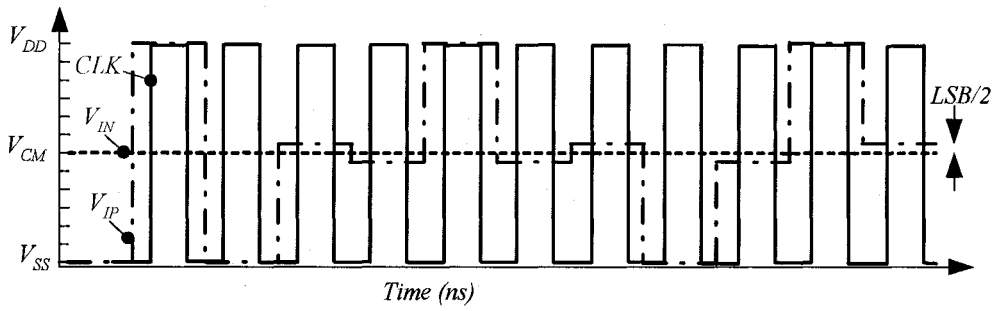


**Figure 6.19:** Waveform used for the dynamic testing of the comparator.

### *6.3.2 Low-voltage rail-to-rail input/output opamp*

The input common-mode range and the output voltage swing of the opamp circuit proposed in Figure 5.1 have been simulated under a supply voltage of 1 V to

confirm our proposal and the results are presented in Figures 6.20 and 6.21 respectively. An almost rail-to-rail input and output swing is obtained. The frequency response and step input response of the circuit are presented in Figures 6.22 and 6.23, respectively. A 26.6 MHz unity gain frequency with a 67-degree phase margin was obtained under load conditions of 5 pF and 20 kΩ. The overall circuit power dissipation is 400 μW.

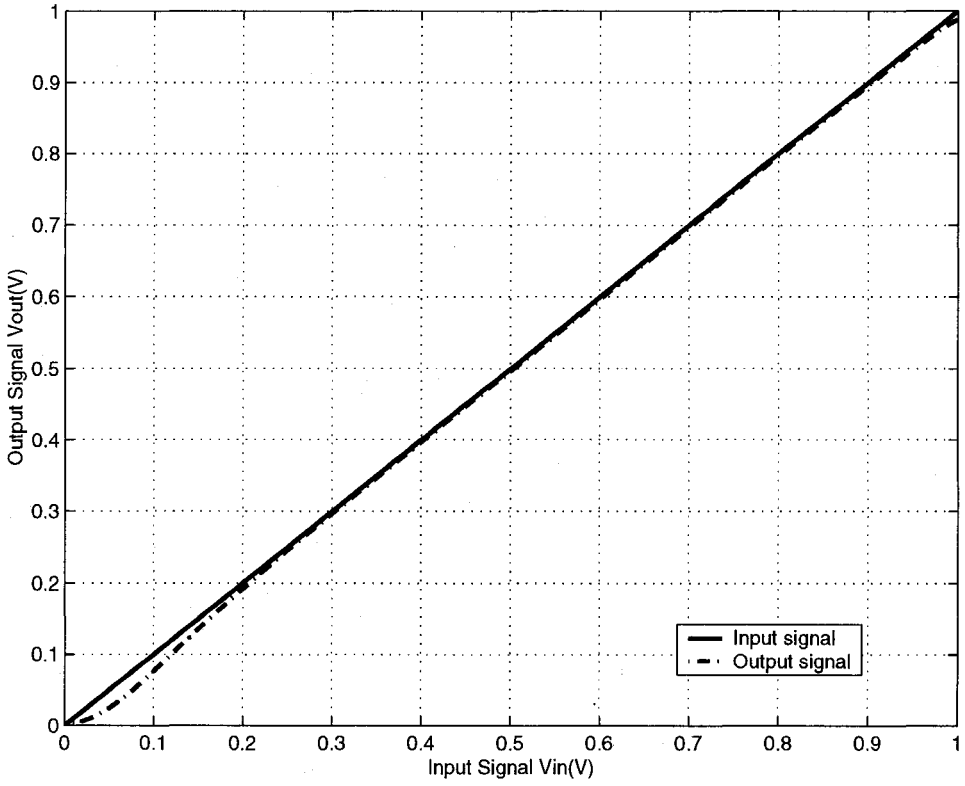


**Figure 6.20:** Simulated opamp input CMR.

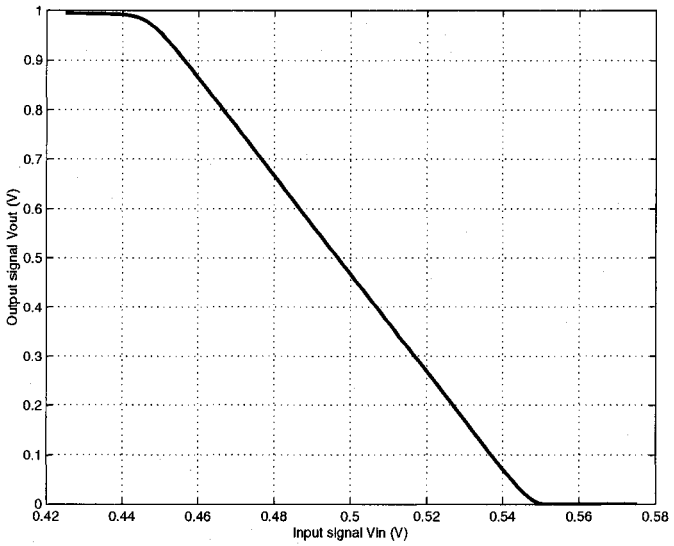


**Figure 6.21:** Simulated opamp output swing.

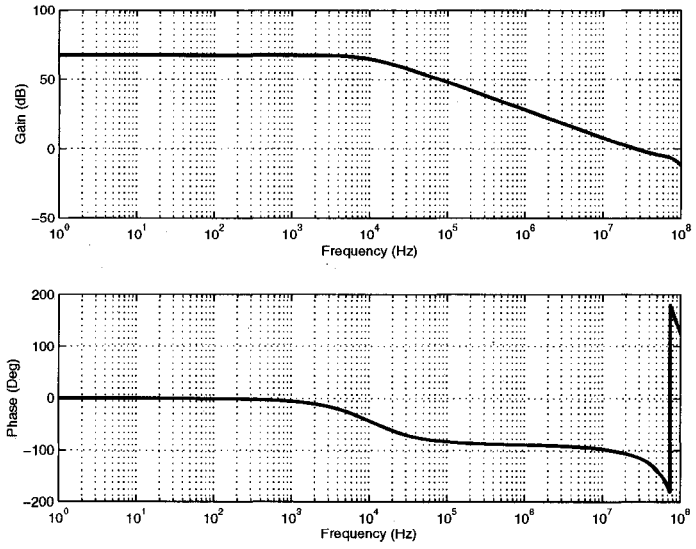


**Figure 6.22:** Simulated opamp Frequency response.

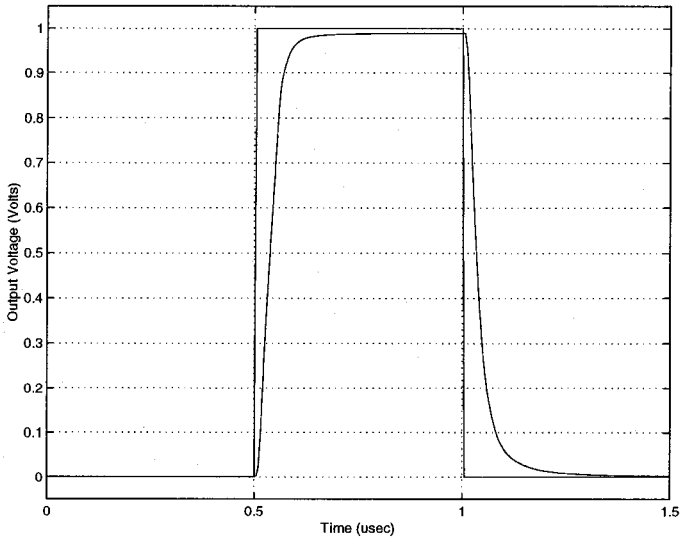


**Figure 6.23:** Simulated opamp step input response.

### *6.3.3 Low-voltage rail-to-rail successive approximation ADC*

Only functional simulation has been performed on the R-2R DAC-based successive approximation ADC of Figure 5.13.

The regenerative latch-based rail-to-rail comparator (Figure 5.10) used in this ADC was first simulated using the critical waveform reported in Figure 6.19 to check its true resolution. In practical implementation, this waveform can be generated using an arbitrary waveform generator or by using the method reported in [DUF99]. The simulated comparator performance using $V_{DD}$ = 1.0 V, a switching voltage overdrive of ± 0.1220 mV (which corresponds to a ± 0.5 LSB of a 12 bit precision) and a 16.67 MHz clock signal with an inverter as a load is shown in Figure 6.24.

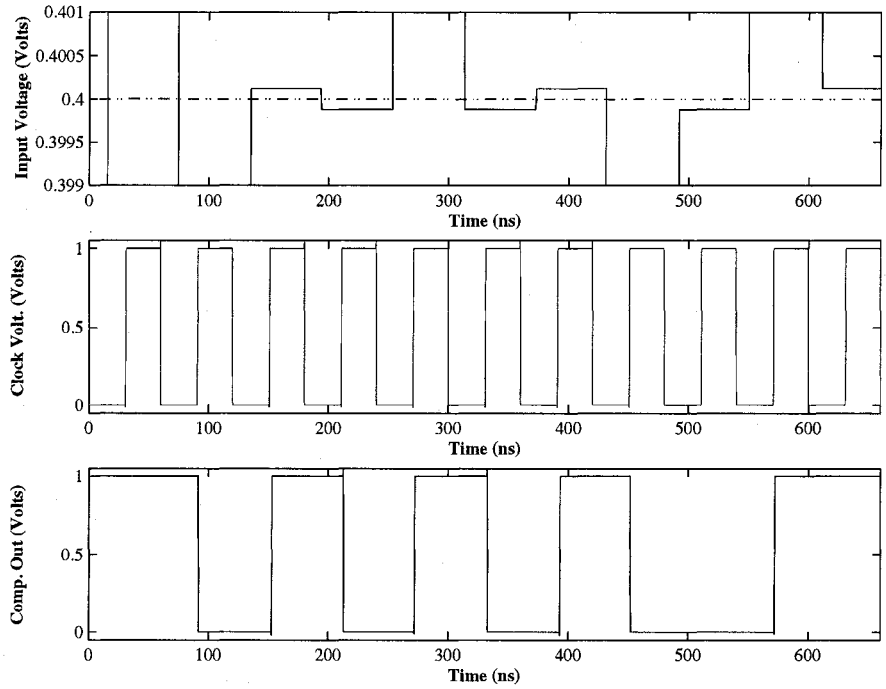


**Figure 6.24:** Simulated rail-to-rail input regenerative latch-based comparator.

The functional ADC simulation has been performed after setting the sample-and-hold input signal respectively to $V_{DD}$ and $0.125 \times V_{DD}$. The simulation performed using a 2.22 MHz clock signal corresponding to an approximated sampling speed of 200 kS/s, is shown in Figure 6.25. The functional simulation displays how well the DAC output tracks its corresponding sample-and-hold circuit output. This sampling speed is dictated by the best achievable performance from the sample-and-hold circuit as reported in section 6.2.4.

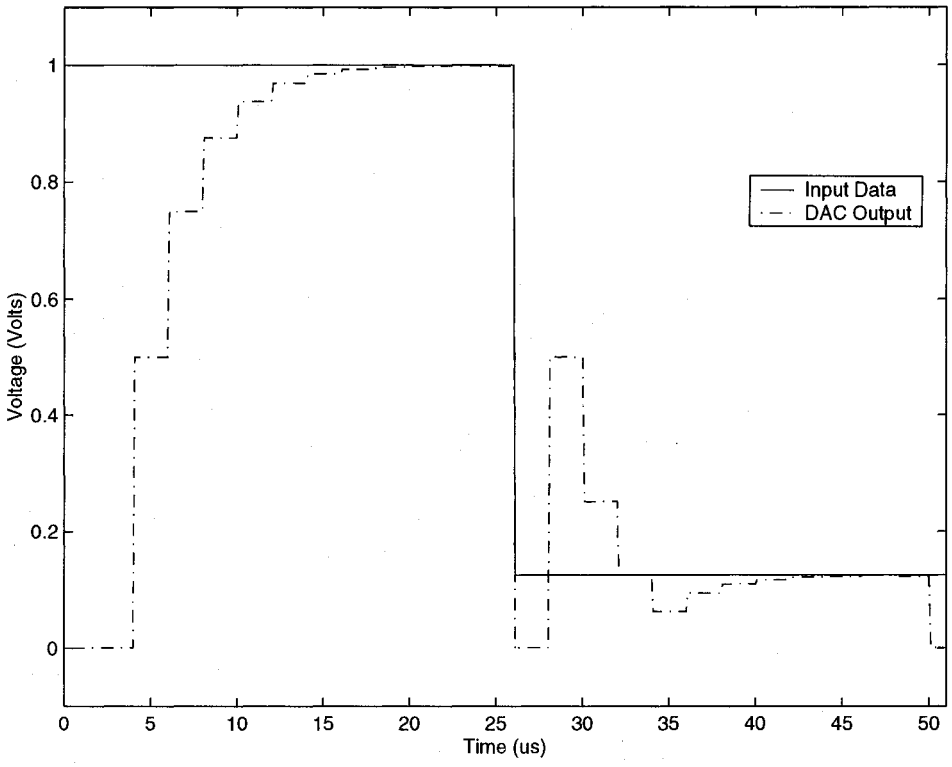


**Figure 6.25:** Simulation of two conversion cycles.

In this chapter both experimental and simulated results of the proposed low-voltage almost rail-to-rail input common-mode range analog building blocks have been reported. Most of the proposals have been experimentally verified and checked. The following chapter will summarize our main contributions and introduce further extension of this work.

# *Chapter 7*

# *CONCLUSION AND RECOMMENDATIONS*

*"I never see what has been done ... I only see what remains to be done."*
*- Marie CURIE*

The history of IC design is one of constantly changing silicon technology. The bipolar transistor used to rule the IC world has now been replaced by the CMOS transistor to the extent that some universities do no longer teach the use of BJT. The thin film resistor and laser wafer trimming that were once the mainstay of the analog business are considered relics of the past. High quality passive components of any kind are frowned upon in modern design, and engineers strive to content themselves with plain, digital CMOS capabilities. Likewise, the reductions in supply voltage and the increasing demand for low power have caused a virtual revolution in circuit architecture.

Data converters are inherently mixed signal circuits and present the same challenges in smaller scale. The main challenges in data converter design at low voltage operation conditions are noise, signal swings, accuracy, sampling linearity, conversion speed, mixed-signal issues, design development and so on.

This research is focused on the issues associated with low-voltage analog building blocks for ADCs. Our purpose was to search for and develop techniques and circuit structures suitable for today's and future low voltage technologies. The main

contributions of our research are summarized below, and followed by recommendations for future research.

## 7.1 Original contributions of this thesis

Here are the main contributions of this thesis:

- A new approach to the design of a CMOS differential latched comparator suitable for low voltage applications. The novel approach makes use of the well-known constant-gm rail-to-rail input stage used in amplifiers.
- A sample-and-hold circuit based on a novel implementation of the boot-strapped low-voltage analog CMOS switch. The heart of this circuit is a new low-voltage and low-stress CMOS clock voltage signal booster. Through the use of a dummy switch, the charge injection induced by the bootstrapped switch is greatly reduced resulting in improved sample-and-hold accuracy.
- A design strategy for a rail-to-rail input/output operational amplifier. The circuit makes use of a novel level shifting technique of the input signal and a dynamically biased class AB output stage based on a switched-capacitor configuration.
- The implementation of two successive approximation analog-to-digital converter architectures suitable for low-voltage and medium resolution applications.

## 7.2 Recommendations for future work

In the future, both digital and analog circuits will clearly need a finite amount of voltage to represent signals. Furthermore, a minimum amount of margin is fundamentally necessary for noise. Thus, what is the minimum voltage required to operate these circuits? Due to current leakage considerations, a threshold voltage less than 0.4 V is unlikely. To maintain circuit speed, some margin of overdrive voltage is required beyond 0.4 V. This is true for both digital and analog circuits as current is a function of $V_{GS}$-$V_{th}$. Therefore, it is possible that both circuit types scale together. However, due to the unscalability of $V_{th}$ it is not sure that voltage supplies will drop below 0.6 V.

### *7.2.1 Circuit reliability test*

An interesting continuation of this work would be to test the reliability of the proposed bootstrapped techniques. The principle of operation is sound, but actual verification would prove the concept. The experimental prototype was fully characterized for performance at 1 V and 0.65 V. However, lifetime extrapolation of the device was beyond the scope of this research. This could be done with a reliability simulator of the bootstrap circuit, such as Berkeley Reliability Tool [HU92], and with the actual accelerated stressing of a statistically significant large population of test devices.

### *7.2.2 Fully differential implementation*

Fully differential topologies are a necessity in any modern mixed-signal CMOS integrated design, including switched-capacitor circuit. The benefits of a fully differential design can be summarized and listed as follows: input common mode

voltage remains at a defined level $V_{CM}$, a doubling in the output swing leading to an increase in the dynamic range of the circuits, reduction in harmonic distortion since the even-order harmonic distortion terms are canceled and finally the substrate and coupled noise rejection.

Further improvements of the circuit techniques presented in this research would be the extension of the topology to fully differential implementation followed by an experimental verification.

### *7.2.3 Extension to other low-voltage A/D conversion*

It would be interesting to complete the experimental validation of the proposed successive approximation ADC described in Chapter 5. Due to the market evolution, special efforts could be devoted in applying the proposed circuit techniques to the synthesis of other low-voltage A/D converters such as oversampling $\Sigma\Delta$, algorithmic, pipeline to name just a few.

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# *Appendix A*

# *CURRENT DIVISION PRINCIPLE*

A technique for dividing currents (or voltages) very accurately and linearly is useful for various kinds of analog signal processing such as controllable attenuation, analog-to-digital and digital-to-analog conversion. A common technique is based on resistors or capacitors for the linear and accurate division of current (or voltage) while using MOS transistors as switches or amplifying elements [MCC75], [LEE84]. Here the same MOS transistor is used for both the signal division as well as switching functions, thus eliminating the need of capacitors or resistors. Although a MOS transistor exhibits a non-linear relationship between current and voltage (even in the linear region), we are demonstrating that the current division is inherently linear.

A general MOST model is described in Section A.1. In Section A.2, the basic of the current division will be shown followed by the proof of the technique.

## A.1 General MOS transistors model

Figure A.1 shows a cross section of a MOS transistor. For purpose of clarity, we will confine the explanation to n-channel transistors, but the model also applies as well to p-channel MOSTs.

We will start by defining the channel voltage $V_C$ (x) at a certain position x in the channel

from the source voltage $V_S$ (x = 0) to the drain voltage $V_D$ (x = L). The current at an arbitrary location x in the channel can be induced by both the drift and diffusion. If the inversion layer current at x is denoted by I(x), we have [TSI99]:

$$I(x) = I_{drift}(x) + I_{diff}(x) \tag{A.1}$$

The current due to drift is proportional to the local channel density $Q_C$, the electron mobility μ, the local electric field along the channel $dV_C/dx$, and the channel width W:

$$I_{drift}(x) = -W\mu Q_C \frac{dV_C}{dx} \tag{A.2}$$

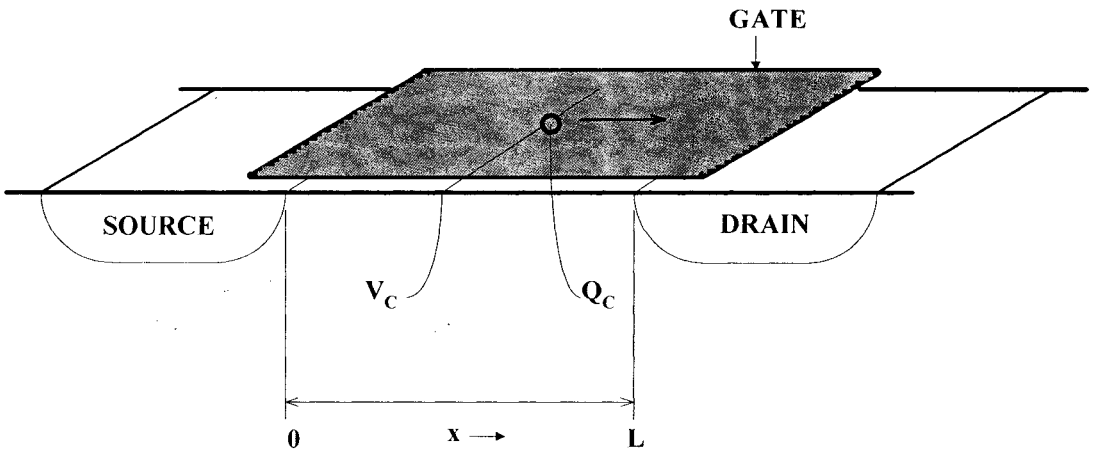


**Figure A.1:** Cross-view of a MOS transistor.

The current due to diffusion is proportional to the electron mobility μ, the channel width W, the thermal voltage kT/q, and the derivative of the charge density $Q_C$, with respect to the position x:

$$I_{diff}(x) = W\mu \frac{kT}{q} \frac{dQ_C}{dx} \tag{A.3}$$

Substitution of (A.2) and (A.3) into (A.1) leads to:

$$I(x) = W\mu\left[-Q_C\frac{dV_C}{dx} + \frac{kT}{q}\frac{dQ_C}{dx}\right] \tag{A.4}$$

As the current is constant along the channel (quasi steady state), integration from the source to drain leads to the following equation:

$$IL = W\int_{x=0}^{x=L} -\mu\left[Q_C\frac{dV_C}{dx} - \frac{kT}{q}\frac{dQ_C}{dx}\right]dx \tag{A.5}$$

Changing the running variable to the channel voltage $V_C$ and dividing by L yields the following expression for the current drain $I_D$ (= -I):

$$I_D = (W/L)\int_{V_C=V_S}^{V_C=V_D} f(V_G, V_C)dV_C \tag{A.6}$$

with

$$f(V_G, V_C) = -\mu Q_C + \mu\frac{kT}{q}\frac{dQ_C}{dV_C} \tag{A.7}$$

This expression clearly shows the symmetry of the MOS device (interchanging source and drain results in a drain current of equal magnitude but of opposite sign) and the scalability with the device dimensions W and L. The function f ($V_G$, $V_C$) can be a very complicated one, including effects like mobility reduction and body effect. In general though, this expression can be very accurate, especially in the linear region [TSI99]. The influences of the drain on the device current in saturation however, due to the channel-length shortening and drain-induced barrier lowering, are poorly modeled. For our purpose here only the form (A.6) is important and not the specific value of $I_D$ for some $V_G$, $V_S$, and $V_D$. A graphical representation of (A.6) is shown in Figure A.2.

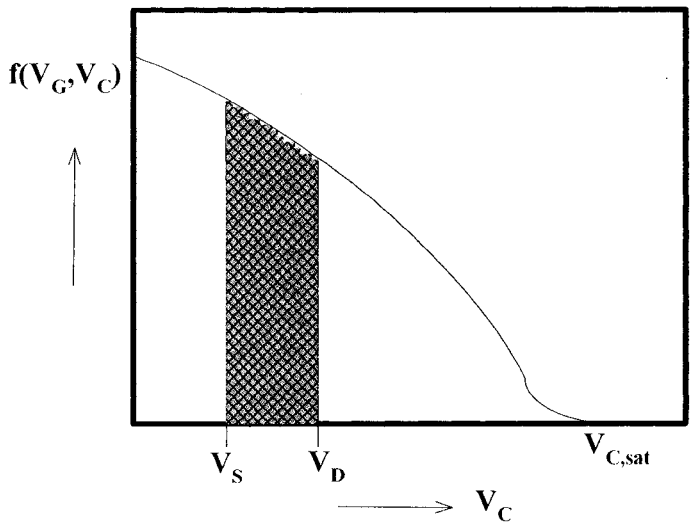


**Figure A.2:** Function f ($V_G$,$V_C$) as a function of the channel voltage $V_C$.

The curve shows the function f($V_G$,$V_C$), for a certain voltage $V_G$, as a function of the channel voltage $V_C$. Following (A.6), integration of this function, by the channel voltage $V_C$ running from the source voltage $V_S$, to the drain voltage $V_D$, and multiplying the result with the ratio (W/L), leads to the drain current $I_D$. Therefore, apart from the factor (W/L), the shaded area represents the current through the MOS device.

In the strong inversion region, a first order approximation (i.e. neglecting the second term of (A.7), assuming constant mobility and linear dependence of $Q_C$ of $V_C$), the function f($V_G$,$V_C$) in Figure A.2, would be a straight line and integration would lead to an ideal quadratic voltage-current relationship. This approach gives a simple MOS model for hand calculation. The bending of the f($V_G$,$V_C$) curve toward the lower value of $V_C$ is primarily caused by mobility reduction. The deviation from the straight line in the vicinity of $V_{C,sat}$ is caused by weak inversion. In this region, the first term in (A.7)

becomes negligible and, in the second term, $Q_C$ is an exponential function of $V_C$, leading to an exponential voltage-current relationship.

## A.2 Basic principle of the current division technique

The basic principle of the current division technique is shown in Figure A.3.

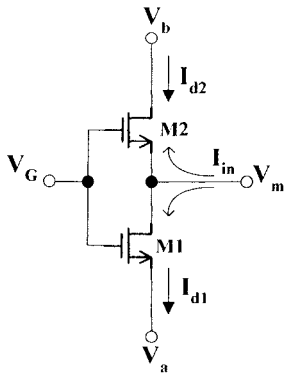


**Figure A.3:** Basic principle of the current division.

Both transistors have the same gate voltage (with respect to the substrate) potential. Voltages $V_a$ and $V_b$ are dc voltages and may have any value as long as the transistors are in the on-state. A current $I_{in}$ flowing into or out of the circuit will be divided into two parts. One part flowing into the node connected to $V_a$ and the other flowing into the node connected to $V_b$. Figure A.4 shows the graphical representation of the current through the transistor of Figure A.3.

As both transistors share the same gate voltage $V_G$, we use the same curve for the function $f(V_G,V_C)$ according to (A.7) as a function of the channel voltage $V_C$. Moreover, as the drain voltage of the lower transistor equals the source voltage of the upper

transistor, the areas representing the currents through each transistor are always adjacent.

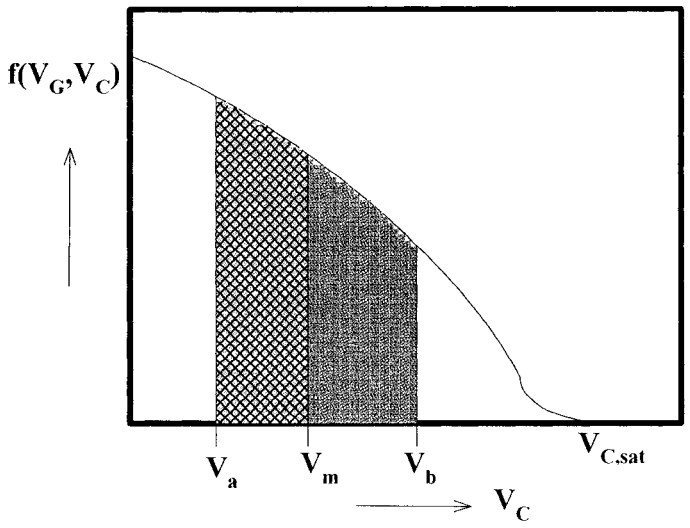


**Figure A.4:** Drain current of the two MOSTs of Figure A.3.

If an input current is applied (Figure A.3), the voltage $V_m$ at the input node will be a (non-linear) function of the input current $I_{in}$, where $V_m = V_m(I_{in})$. Let $V_{m1}$ be the initial input voltage and let $V_{m2}$ be the input voltage when an input current has been applied. From Figure A.5, we can see that, apart from the factor $(W_1/L_1)$, the increase of the current through the lower transistor, $\Delta I_{d1}$, is represented in the Figure by a simple shaded area. Similarly, apart from the $(W_2/L_2)$, the decrease in the current through the upper transistor, $-\Delta I_{d2}$, is represented by the same area.

This means that, although $V_m(I_{in})$ is a non-linear function of $I_{in}$, the ratio:

$$\frac{\Delta I_{d1}}{\Delta I_{d2}} = -\left(\frac{W}{L}\right)_{M1} \Big/ \left(\frac{W}{L}\right)_{M2} \tag{A.8}$$

is independent of $I_{in}$ and dependent of the geometry of the devices only. As:

$$I_{in} = \Delta I_{d1} - \Delta I_{d2} \tag{A.9}$$

then, it follows that:

$$\frac{\Delta I_{d1}}{I_{in}} = \frac{1}{1+\left(\frac{W}{L}\right)_{M1}\Big/\left(\frac{W}{L}\right)_{M2}} \tag{A.10}$$

$$\frac{\Delta I_{d2}}{I_{in}} = \frac{1}{1+\left(\frac{W}{L}\right)_{M1}\Big/\left(\frac{W}{L}\right)_{M2}} \tag{A.11}$$

This implies that the current division is inherently linear and insensitive to second-order effects like mobility reduction and body effect and valid in all operating regions of a MOS transistor.

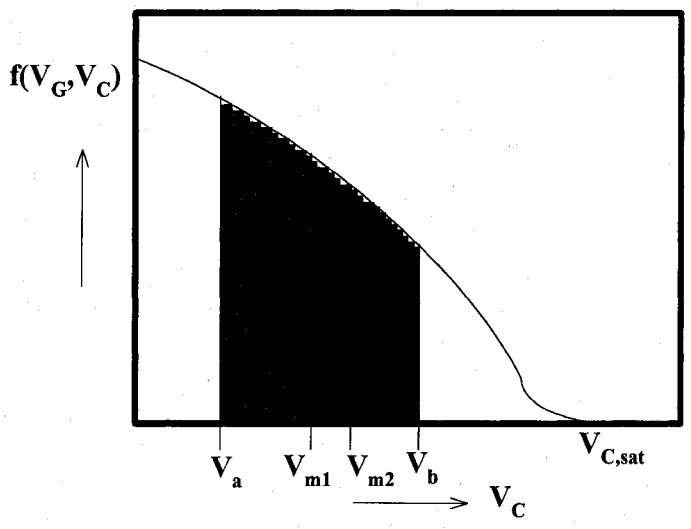


**Figure A.5:** Drain current of the two MOS transistors before and after a current $I_{in}$ is injected in the input.